Empowered by Innovation

NEC

High-Performance Microcontrollers

V850 Series

Empower your creativity

V850

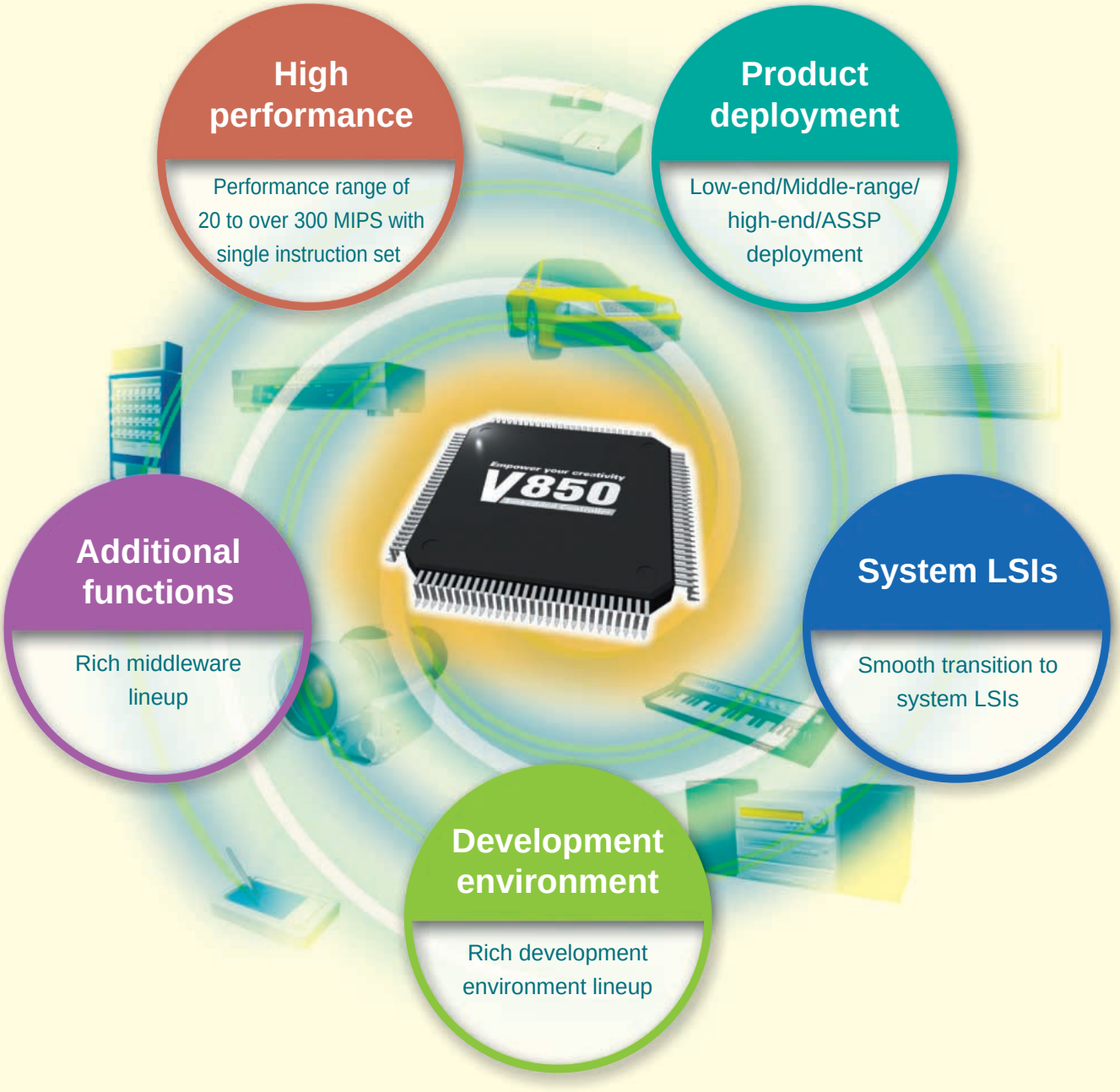
Embedded Controller

Empower your creativity

V850

Embedded Controller

The V850 Series of high-performance microcontrollers answers many different application system needs. It realizes superlatively low power consumption and low noise while offering high performance and a wide array of functions.
The broad V850 product lineup provides optimum solutions for the next-generation systems of customers.



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Roadmap/Features

V850 Series Product Roadmap

Continuously evolving V850 Series through an expanding product lineup

V850E2 core 200 to 400 MHz

CPU core release completed
Product deployment under planning

V850E1 core

150 MHz @ 215 MIPS

High-end lineup

High performance: On-chip MEMC/DMA

- Frequency: 33 to 150 MHz
- Memory size: ROM: ROM-less to 512 KB
  RAM: 4 to 128 KB
- PKG: 100 to 240 pins (QFP & FBGA)

V850 core

33 MHz @ 38 MIPS

Middle-range lineup

Realization of low EMI noise

- Frequency: 20 to 34 MHz
- Memory size: ROM: ROM-loss to 640 KB
  RAM: 4 to 48 KB
- PKG: 100 to 144 pins (QFP & FBGA)

V850ES core

20 MHz @ 29 MIPS

Low-end lineup

High cost-performance

- Frequency: 20 MHz
- Memory size: ROM: 64 to 256 KB
  RAM: 4 to 16 KB
- PKG: 64 to 144 pins (QFP)

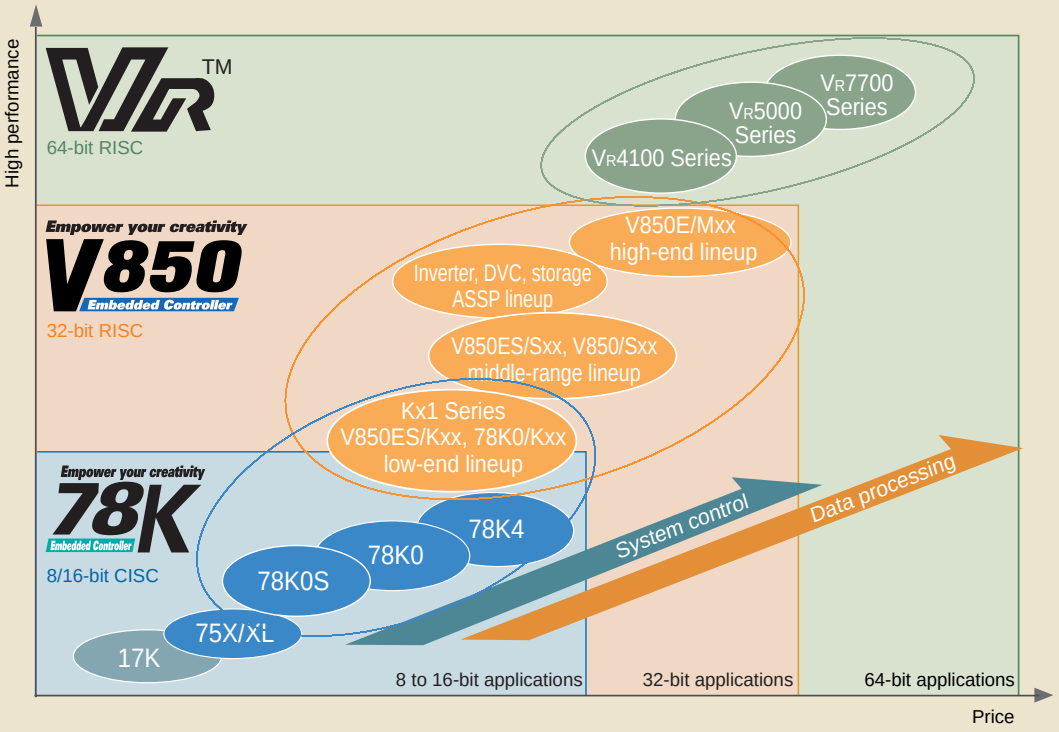
ASSP lineup

Inverter control
DVC control
Car audio control
Power meter control
Dashboard control

- Frequency: 16 to 64 MHz
- Memory size: ROM: ROM-less to 640 KB
  RAM: 4 to 48 KB
- PKG: 64 to 257 pins
  (QFP & FBGA)

Standard lineups | Field-specific lineups

NEC Electronics Microcontroller Deployment



Upward compatible instruction sets

Set Application Examples

The V850 Series is suitable for various application fields and raises the commercial value of customer systems.

Automotive	Engines, dashboards, power steering, ABS
Audio	Car audio, portable audio, component stereo systems
Portable devices	PDA, IC recorders
Camera	DVC, DSC, SLR cameras
Computer peripherals	Laser-beam printers, inkjet printers, scanners, fax machines
Home appliances	Air conditioners, refrigerators, washing machines, microwave ovens
Industrial equipment	Industrial motors, control equipment, vending machines, power meters
Video and recording equipment	DVD players, D-VHS, industrial cameras
Other	Electronic instruments, electric bidets, toys, learning devices, remote controllers, etc.

5 Keys of V850

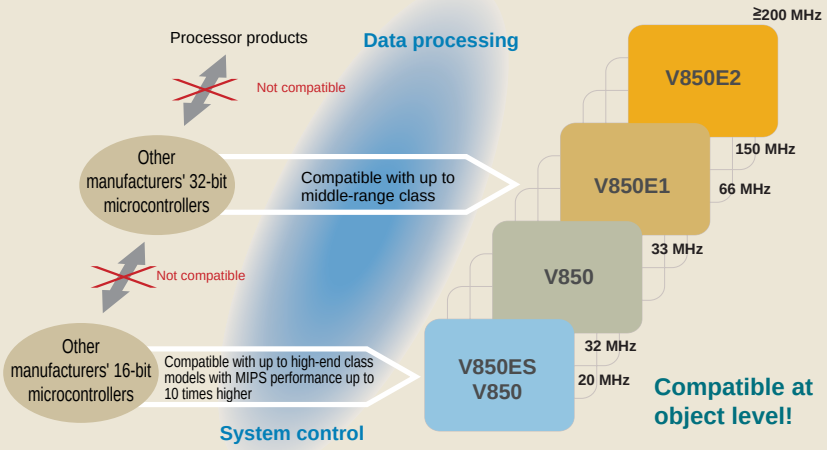
5 points supporting the high performance of the V850 Series

High performance

Performance ranging from 20 to over 300 MIPS with single instruction set

High performance

- Compared to 8-/16-bit microcontroller, offer a MIPS performance 10 or more times higher for the same frequency, and 2 to 3 times higher at the actual application level (based on NEC evaluation)
- System operation at frequencies 1/2 to 1/3 those of 8-/16-bit microcontrollers is enabled, contributing to lowering system power consumption.
- The V850 core, V850ES core, V850E1 core, and V850E2 core are upward compatible at the object level.

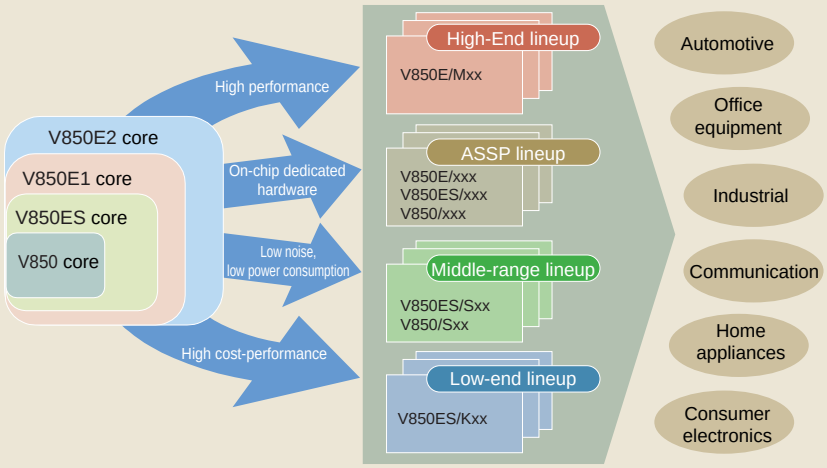


Product lineup

Low-end/Middle-range/High-end/ASSP deployment

Product lineup

- Low-end lineup: Kx1 Series of general-purpose microcontrollers for 16 to 32-bit market designed for high cost-performance.
- Middle-range lineup: Low noise, low power consumption, large-capacity memory lineup, low-voltage operation support
- High-End lineup: Designed for high performance, on-chip memory controller and DMA
- ASSP lineup: Field-specific product lineup, on-chip dedicated hardware

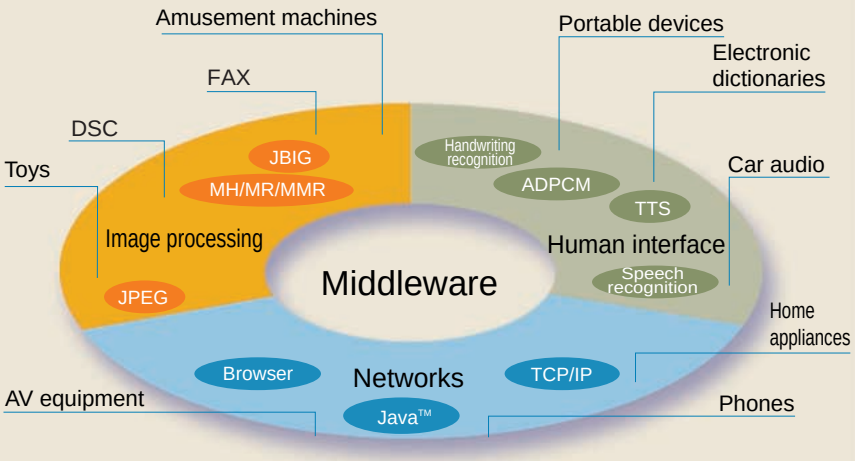


Additional functions

Rich middleware lineup

Additional functions

- Realization of systems with high added value through the addition of supplementary functions to existing systems via middleware
- Realization of functions heretofore realized with peripheral ICs through V850 + middleware, reducing development time and reducing system costs
- Rich lineup of video, audio, network-related, and other middleware tuned for V850 Series

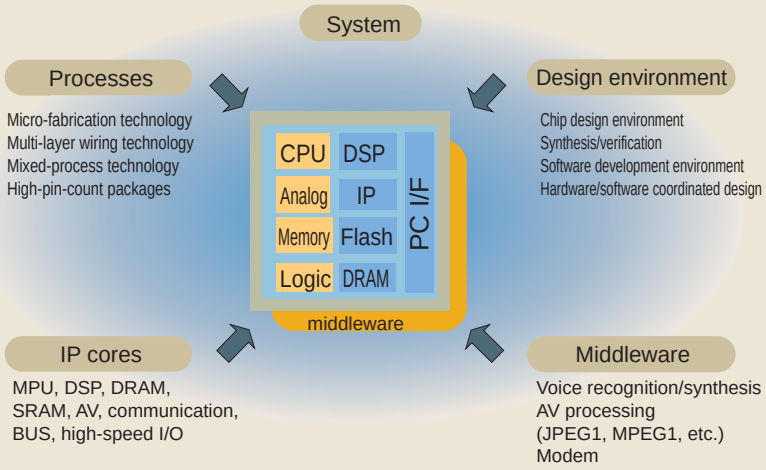


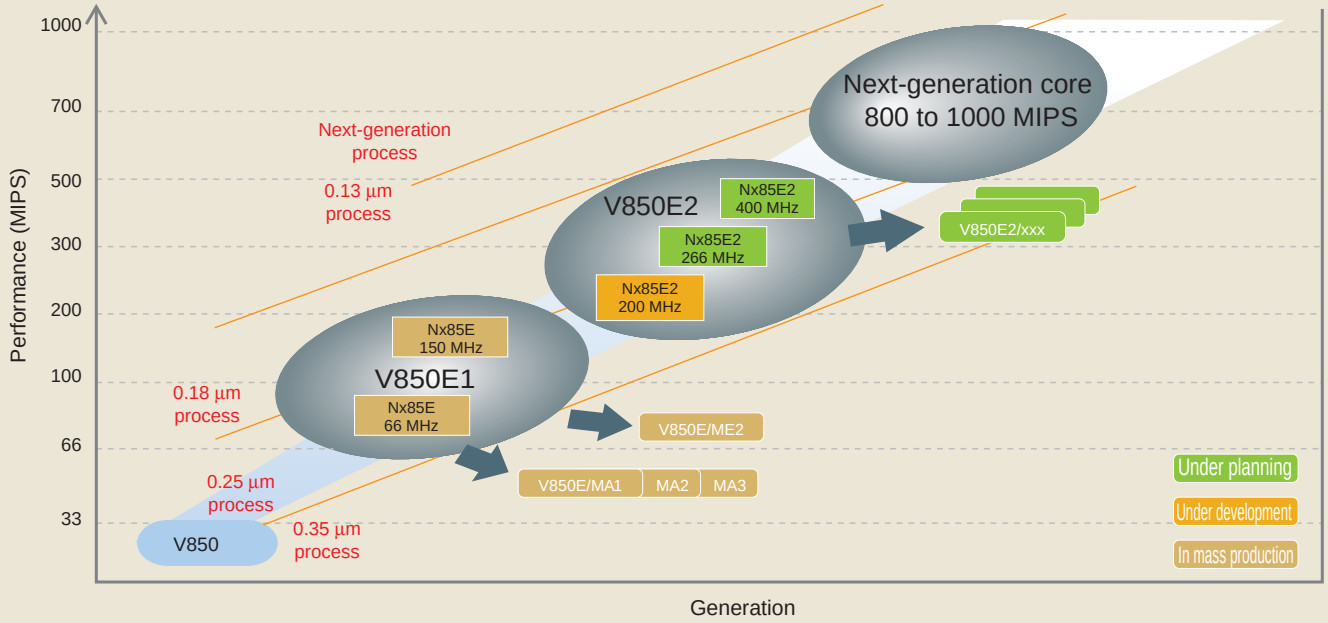
System LSI

Smooth transition to system LSIs

System LSI

- The V850 Series is also being actively expanded for ASIC CPU cores, realizing smooth transition to system LSIs
- The following elements essential for system LSIs are provided on a timely basis:
  - <1> Leading-edge process technology
  - <2> High-performance CPU core
  - <3> Rich lineup of IP cores
  - <4> Top-down design environment
  - <5> Flexible application design



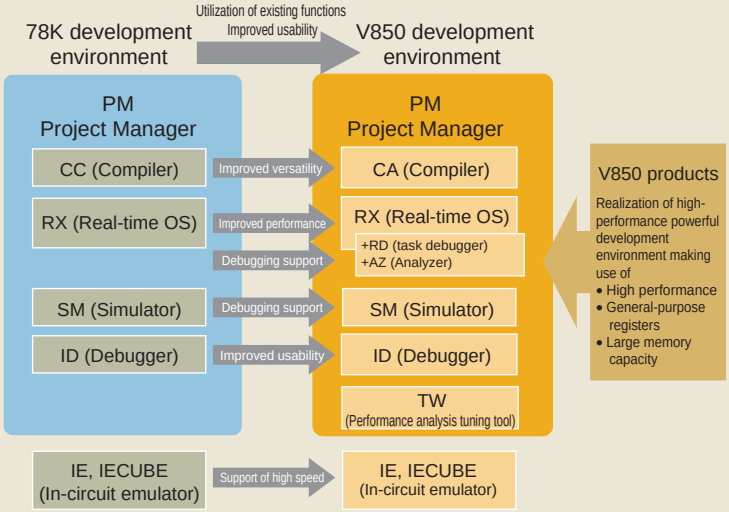


Development environment

Rich development environment lineup

Development environment

- IECUBE™, a low-cost high-performance emulator, and N-Wire CARD, an ultra-low cost on-chip emulator are available
- Realization of better connectivity with target boards, addition of GUI customization function, improved online help, etc.
- Realization of shorter development TAT through support of quick and accurate software development via a rich development environment lineup featuring easy operation and sophisticated functions



Product Lineup

Low-End Lineup

Kx1 Series of general-purpose microcontrollers for 16 to 32-bit market designed for high cost-performance

Under planning
Under development
In mass production

NEXT Generation

V850ES/KE1+	V850ES/KF1+	V850ES/KG1+	V850ES/KJ1+
64-pin version	80-pin version	100-pin version	144-pin version

Single-power-supply flash
On-chip POC/LVI
On-chip debugging function
DMA function (only KG1+, KJ1+)

V850ES/KE1	V850ES/KF1	V850ES/KG1	V850ES/KJ1
64-pin version	80-pin version	100-pin version	144-pin version

8-bit microcontrollers
78K0/Kxx
78K0S/Kxx

- Rich memory and package lineup
- Large array of on-chip peripheral functions common with 78K0/Kx1 of 8-bit microcontrollers
- Low EMI noise design
- Development environment usable in common for all series
- Wide voltage range support (2.7 to 5.5 V)
- Single-power-supply flash lineup (self programming, EEPROM™ emulation support)

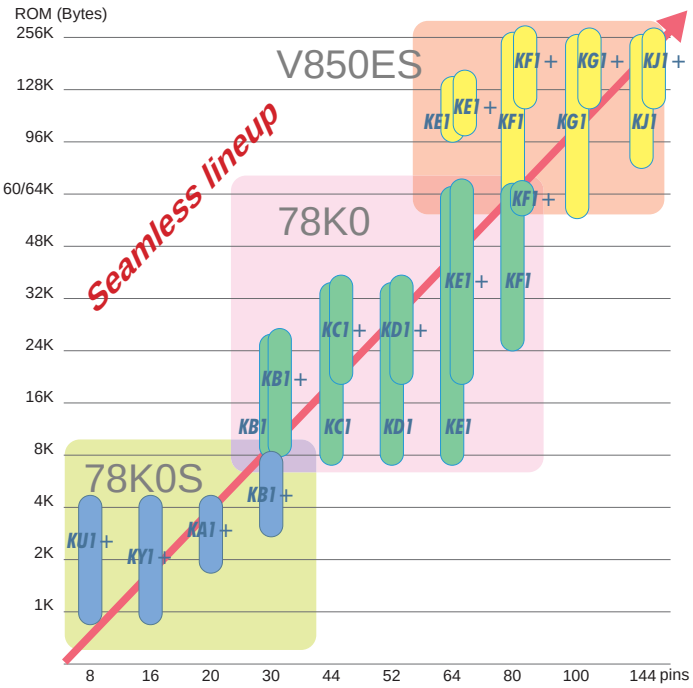
Kx1+ features

Kx1+ are microcontrollers featuring additional functions.

	V850ES/Kx1		V850ES/Kx1+
Runaway detection function	Watchdog timer running on main clock	plus	High-reliability watchdog timer operating with uninterruptible Ring OSC
Voltage detection circuit	None	▶	On-chip voltage detection circuit (LVI: variable detection voltage)
Reset functions	External reset, WDT reset	plus	•On-chip reset detection circuit (POC: Fixed voltage) •Also possible with voltage detection circuit (LVI: Variable detection voltage)
DMA function	None	plus	4 on-chip channels (KG1+, KJ1+)
Oscillation stabilization time reduction	Fixed at reset release	▶	Can be reduced with optional function
A/D converter	Conversion time 14 µs (min.) Successive approximation mode	▶	Conversion interval of 3 µs (min.) Successive approximation, scan mode
LIN bus interface	No hardware	▶	1 hardware channel for each product

Kx1 Series lineup

Rich memory & package lineup

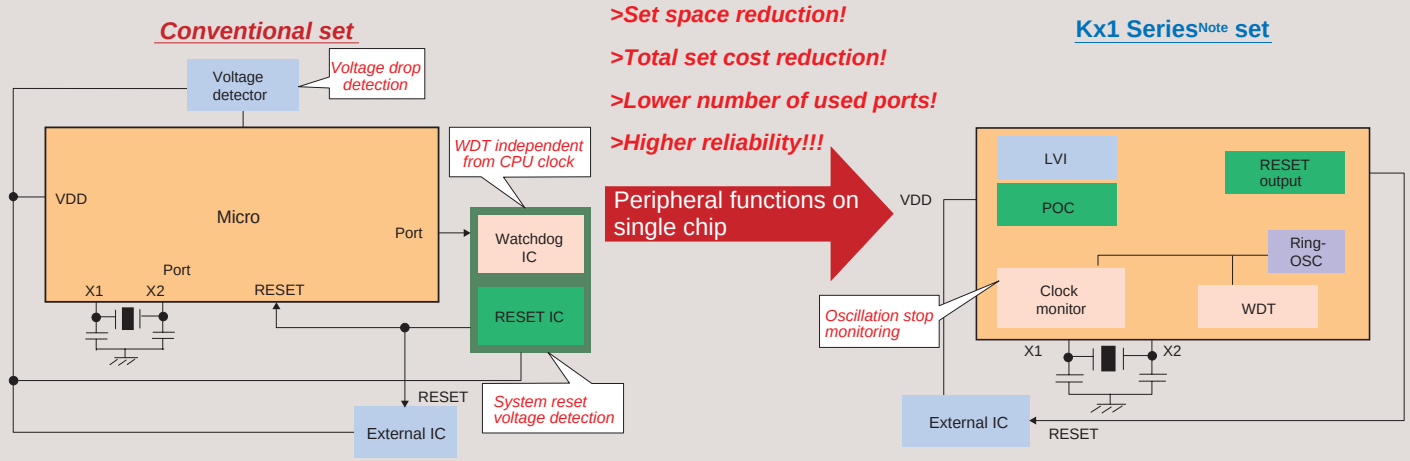


◆Product specifications◆

Item	V850ES/Kx1			
	KE1	KF1	KG1	KJ1
CPU core	V850ES			
Performance	29 MIPS (@ 20 MHz)			
Maximum operating frequency	20 MHz (main clock) 32.768 kHz (subclock)			
Internal flash memory	128 KB	256 KB/128 KB		
Internal mask ROM	128 KB	256 KB/128 KB/96 KB/64 KB		128 KB/96 KB
Internal RAM	4 KB	12 KB/6 KB/4 KB	16 KB/6 KB/4 KB	16 KB/6 KB
Power supply voltage	4.5 V to 5.5 V @ 20 MHz 4.0 V to 5.5 V @ 16 MHz 2.7 V to 5.5 V @ 10 MHz			
External bus	-	Address: Multiplexed	Address: Multiplexed/separate	
		Data: 8/16-bit		
Timer/counter	16-bit×2 ch	16-bit× 2 ch (256 KB: 3 ch)	16-bit×4 ch (256 KB: 5 ch)	16-bit×6 ch (256 KB: 7 ch)
	8-bit×5 ch			
	WDT×2 ch			
	Watch timer×1 ch			
Serial interface	CSI×2 ch, UART×2 ch I²C×1 ch*	CSI×2 ch, UART×2 ch I²C×1 ch* CSI with automatic transfer function×1 ch	CSI×2 ch, UART×2 ch I²C×1ch* CSI with automatic transfer function×2 ch	CSI×3 ch, UART×2 ch UART/I²C×1 ch*, I²C×1 ch* CSI with automatic transfer function×2 ch
A/D converter	10-bit×8 ch			10-bit×16 ch
D/A converter	-		8-bit×2 ch	
DMA controller	-			
Other peripheral functions	ROM correction function, real-time output, key return function			On-chip debug function, ROM correction function, real-time output, key-return function
I/O	51	67	84	128
Power consumption (mask version, Typ.)	150 mW (20 MHz @5V)			
Package	64-pin TQFP(12×12 mm) 64-pin LQFP(10×10 mm)	80-pin TQFP(12×12 mm) 80-pin QFP(14×14 mm)	100-pin LQFP(14×14 mm) 100-pin QFP(14×20 mm)	144-pin LQFP(20×20 mm)

* : Only Y products have an on-chip I²C interface.

System cost reduction



Note: V850ES is supported from Kx1+

Common peripheral functions

Large array of peripheral functions common with 8-bit 78K0 Series

	78K0S				78K0												V850ES										
	KU1+	KY1+	KA1+	KB1+	KB1	KB1+	KC1	KC1+	KD1	KD1+	KE1	KE1+	KF1	KF1+	KE1	KE1+	KF1	KF1+	KG1	KG1+	KJ1	KJ1+
ROM size(bytes)	1K 2K 4K	1K 2K 4K	2K 4K	4K 8K	8K	16K 24K	16K 24K	8K 16K 24K 32K	16K 24K 32K	8K 16K 24K 32K	16K 24K 32K	8K 16K	24K 32K 48K 60K	16K	24K 32K 48K 60K	24K 32K	48K 60K	60K	128K	128K	64K 96K 128K	256K	128K 256K	64K 96K 128K	256K	128K 256K	96K 128K	256K	128K 256K
TMP																			1	1		1	1		1	1		1	1
TM0	1	1	1	1	1	1	1	1	1	1	1	1	2	1	2	1	2	2	1	1	2	2	2	4	4	4	6	6	6
TM5					1	1	1	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
TMH	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
TM8			1	1																									
WT							1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
WDT(Powerful WDT)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
WDT																			1	1	1	1	1	1	1	1	1	1	1
DMA																								4					4
CSI					1	1	1	1	1	1	1	1	2	1	2	1	2	2	2	2	2	2	2	2	2	3	3	3	3
Auto CSI															1	1	1				1	1	1	2	2	2	2	2	2
UART						1	1	1	1	1	1	1	1	1	1	1	1		2	1	2	2	1	2	2	2	3	3	2
UART(LIN)			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			1			1			1			1
IIC																			1	1	1	1	1	1	1	1	2	2	2
A/D	4 ch	4 ch	4 ch	4 ch	4 ch	4 ch	4 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch	16 ch	16 ch	16 ch
D/A																								2 ch	2 ch	2 ch	2 ch	2 ch	2 ch
Ring-OSC(8 MHz)	Y	Y	Y	Y																									
Ring-OSC(240 kHz)	Y*	Y*	Y*	Y*	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y*			Y*			Y*			Y*
Sub-OSC								Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
REG.									Y		Y	Y			Y	Y				Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Key return								Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
ROM correction																			Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
Real-time Output																			Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
H.MUL/DIV											Y	Y	Y	Y	Y	Y	Y	Y											
POC/LVI	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y		Y		Y		Y			Y
RESET OUT					Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y		Y		Y		Y			Y
Clock Monitor					Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y		Y		Y		Y			Y

* : Only for WDT/TMH

Common to all products | Common to V850ES products | Common to 78K0 products | Common to 78K0S products

Item	V850ES/Kx1+			
	KE1+	KF1+	KG1+	KJ1+
CPU core	V850ES			
Performance	29 MIPS (@ 20 MHz)			
Maximum operating frequency	20 MHz (main clock) 32.768 MHz (subclock)			
Internal flash memory	128 KB	256 KB/128 KB		
Internal mask ROM	128 KB	256 KB		-
Internal RAM	4 KB	12 KB/6 KB	16KB/6KB	
Power supply voltage	4.5 V to 5.5 V @ 20 MHz 4.0 V to 5.5 V @ 16 MHz 2.7 V to 5.5 V @ 10 MHz			
External bus	-	Address: Multiplexed	Address: Multiplexed/separate	
		Data: 8/16 bits		
Timer/counter	16-bit×2 ch	16-bit×3 ch	16-bit×5 ch	16-bit×7 ch
	8-bit×5 ch			
	WDT× 2 ch			
	Watch timer×1 ch			
Serial interface	CS × 2 ch, LIN compatible UART × 1 ch UART × 1 ch, I²C × 1 ch*	CS I × 2 ch, LIN compatible UART × 1 ch UART × 1 ch, I²C × 1 ch* CSI with automatic transfer function × 1 ch	CS I × 1 ch, LIN compatible UART × 1 ch UART × 1 ch, I²C × 1 ch*, UART/CSI × 1 ch CSI with automatic transfer function × 2 ch	CSI × 2 ch, LIN compatible UART × 1 ch, UART × 1 ch I²C × 1ch*, UART/CSI × 1 ch, UART/I²C × 1 ch CSI with automatic transfer function × 2 ch
A/D converter	10-bit×8 ch			10-bit×16 ch
D/A converter	-		8-bit×2 ch	
DMA controller	-		4ch	
Other peripheral functions	POC/LVI, Ring OSC, clock monitor function ROM correction function, real-time output, key return function			On-chip debug function, POC/LVI, Ring OSC, clock monitor function, real-time output, key-return function
I/O	51	67	84	127 (Y products, 128)
Power consumption (mask ROM version, Typ.)	T.B.D.			
Package	64-pin TQFP (12×12 mm) 64-pin LQFP (10×10 mm)	80-pin TQFP (12×12 mm) 80-pin QFP (14×14 mm)	100-pin LQFP (14×14 mm) 100-pin QFP (14×20 mm)	144-pin LQFP (20×20 mm)

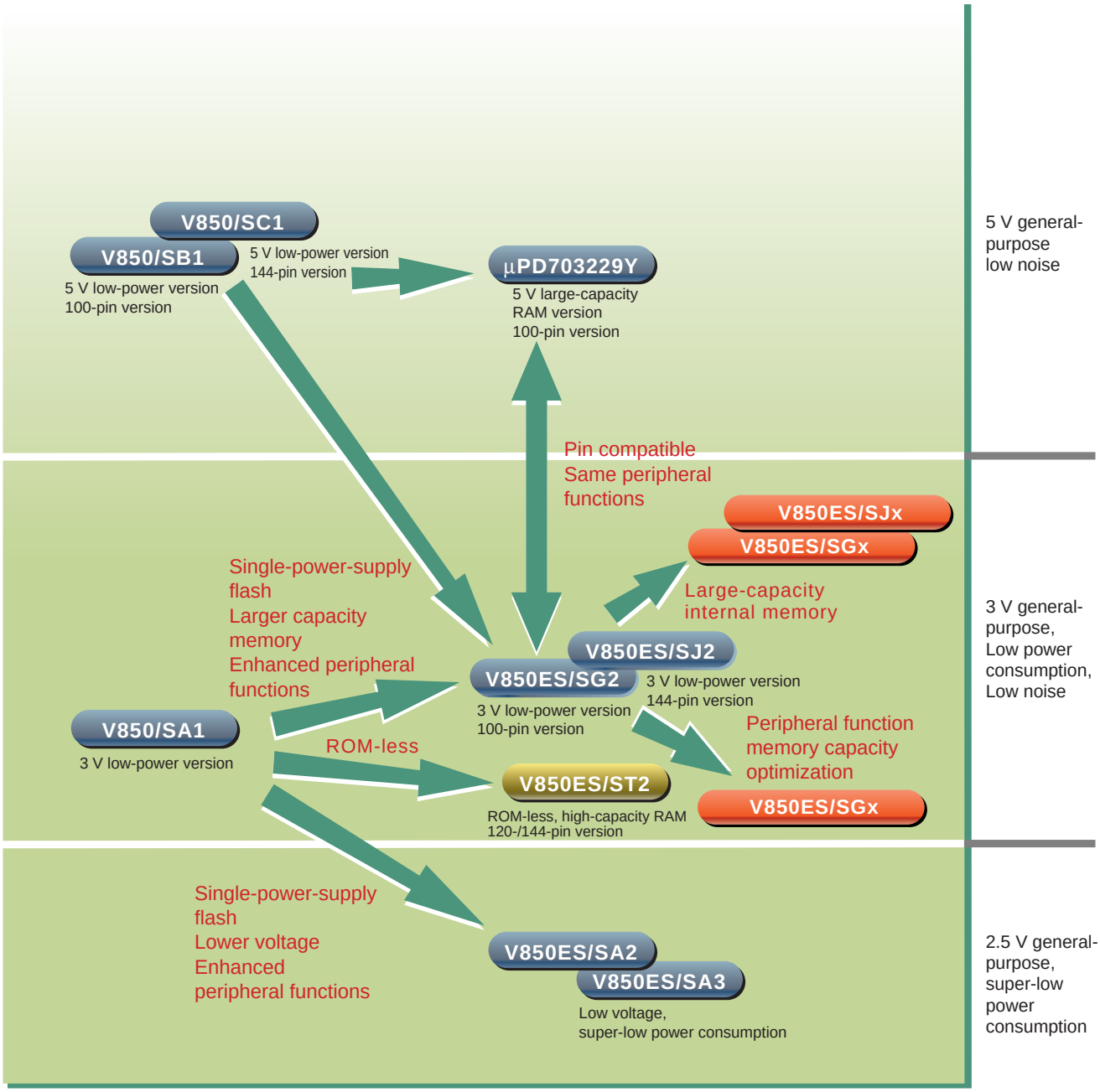
* : Only Y products have an on-chip I²C interface.

Product Lineup

Middle-Range Lineup

Large-capacity memory, 2.5 V/3 V/5 V general-purpose product lineup

Under planning
Under development
In mass production



◆Product specifications◆

Item	V850ES/SAx		V850ES/Sx2		μPD70F3229Y
	SA2	SA3	SG2	SJ2	μPD703229Y
CPU core	V850ES		V850ES		V850ES
Performance	29 MIPS (@ 20 MHz)		29MIPS (@20 MHz)		29MIPS (@20 MHz)
Maximum operating frequency	20 MHz (main clock) 32.768 kHz (subclock)		20 MHz (main clock) 32.768 kHz (subclock)		20 MHz (main clock) 32.768 kHz (subclock)
Internal flash memory	256 KB		640KB/384KB		384KB
Internal mask ROM	256 KB/128 KB	256 KB	640KB/512KB/384KB/256KB	640KB/512KB/384KB	384KB
Internal RAM	16 KB/8 KB	16 KB	48KB/40KB/32KB/24KB	48KB/40KB/32KB	32KB
Power supply voltage	2.2 V to 2.7 V		2.85 V to 3.6 V		3.5 V to 5.5 V (internal) 3.0 V to 5.5 V (external bus)
External bus	Address: Multiplexed/separate Data: 8/16 bits		Address: Multiplexed/separate Data: 8/16 bits		Address: Multiplexed Data: 8/16 bits
Timer/counter	16-bit × 2 ch 8-bit × 4 ch WDT × 1 ch		16-bit×8 ch WDT×1 ch Watch timer×1 ch	16-bit × 11 ch WDT × 1 ch Watch timer × 1 ch	16-bit × 6 ch WDT × 1 ch Watch timer × 1 ch
Serial interface	CSI × 2 ch, CSI/UART × 1 ch UART × 1 ch, CSI/I²C × 1 ch*	CSI × 3 ch, CSI/UART × 1 ch UART × 1 ch, CSI/I²C × 1 ch*	CSI × 3 ch, CSI/LIN compatible UART × 1 ch CSI/I²C × 1 ch* LIN compatible UART/I²C × 2 ch*	CSI × 4 ch, CSI/LIN compatible UART × 1 ch LIN compatible UART × 1 ch, CSI/I²C × 1 ch* UART/I²C × 2 ch*	CSI×1 ch, LIN compatible UART × 3 ch CSI/I²C × 1 ch*
A/D converter	10-bit × 12 ch	10-bit × 16 ch	10-bit × 12 ch	10-bit × 16 ch	10-bit × 12 ch
D/A converter	8-bit×2 ch		8-bit×2 ch		-
DMA controller	4 ch		4 ch		4 ch
Other peripheral functions	Real-time counter (watch function), ROM correction function		On-chip debugging function, CRC circuit, ROM correction function, Ring OSC, low voltage detection circuit, clock monitoring function, automotive bus (IEBus™, aFCAN)Note		On-chip debugging function, ROM correction function, low voltage detection circuit, clock monitoring function
I/O	82	102	84	128	84
Power consumption (mask ROM version, Typ.)	38 mW (20 MHz @ 2.5 V)		59.4 mW (20 MHz @ 3.3 V)	66 mW (20 MHz @ 3.3 V)	100 mW (20 MHz @ 5 V)
Package	100-pin TQFP (14 × 14 mm)	121-pin FBGA (12 × 12 mm)	100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)	144-pin LQFP (20 × 20 mm)	100-pin LQFP (14 × 14 mm)

* : Only Y products have an on-chip I²C interface.

Note Products without automotive bus, products with on-chip IEBus, and products with on-chip aFCAN are available.

Features

V850ES/SG2, SJ2

- Low EMI noise
- 20 MHz @ 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM:640 KB/48 KB, 512 KB/40 KB, 384 KB/32 KB, 256 KB/24 KB (SG2 only)
- Automotive on-chip bus support: IEBus*, aFCAN* (*: Only products with on-chip SG2, SJ2)
- On-chip debugging function
- 100-pin QFP (SG2)/100-pin LQFP (SG2)/144-pin LQFP (SJ2)

V850ES/SA2, SA3

- Min. 2.2 V low-voltage operation (including A/D, D/A converter, flash)
- Low power consumption and high-speed operation during 38 mW @ 2.5 V, 20 MHz operation
- Single-power-supply flash
- ROM/RAM: 256 KB/16 KB (SA2, SA3), 128 K/8 KB (SA2 mask ROM version)
- Thin and compact package support: 100-pin TQFP (SA2)/121-pin FBGA (SA3)

V850/SB1

- Low EMI noise
- Large-capacity memory and large memory selection
- ROM/RAM:512 KB/24 KB, 384 KB/24 KB, 256 KB/16 KB, 128 KB/8 KB
- 100-pin QFP/100-pin LQFP

μPD70F3229Y, 703229Y

- Large-capacity memory
- ROM/RAM:384 KB/32 KB
- 3 V/5 V mixed system support (Internal: 3.3 V/External: 5 V)
- Peripheral functions and pin assignment common with V850ES/SG2
- 100-pin LQFP

V850ES/ST2

- ROM-less version
- On-chip high-capacity RAM (48 KB)
- 3.3 V, 34 MHz operation
- Thin-type, compact type packages supported: 120-pin TQFP/144-pin LQFP

V850/SA1

- Low power consumption and high-speed operation during 66 mW @ 3.3 V, 20 MHz operation
- Large memory selection
- ROM/RAM:256 KB/8 KB, 128 KB/4 KB, 64 KB/4 KB
- 100-pin LQFP/121-pin FBGA

V850/SC1

- Low EMI noise
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Enhanced peripheral functions for SB1
- 144-pin LQFP

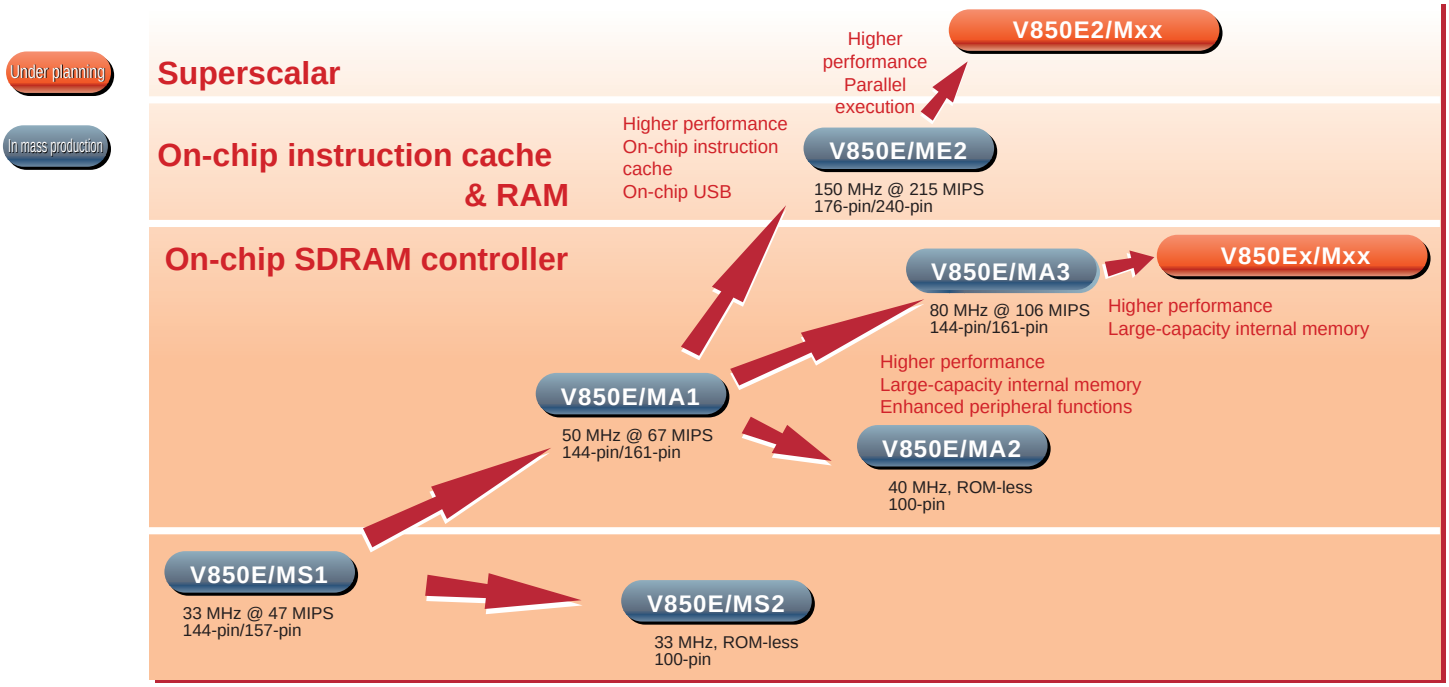
Item	V850/SA1	V850/SB1	V850/SC1	V850ES/ST2
CPU core	V850	V850	V850	V850ES
Performance	23 MIPS (@ 20 MHz)	23 MIPS (@ 20 MHz)	23 MIPS (@ 20 MHz)	-
Maximum operating frequency	20 MHz (main clock) 32.768 kHz (subclock)	20 MHz (main clock) 32.768 kHz (subclock)	20 MHz (main clock) 32.768 kHz (subclock)	34 MHz
Internal flash memory	256 KB/128 KB	512 KB/384 KB/256 KB	512 KB	-
Internal mask ROM	256 KB/128 KB/64 KB	512 KB/384 KB/256 KB/128 KB	512 KB	ROM-less
Internal RAM	8 KB/4 KB	24 KB/16 KB/8 KB	24 KB	48 KB
Power supply voltage	2.7 V to 3.6 V (@ 17 MHz) 3.0 V to 3.6 V (@ 20 MHz)	4.0 V to 5.5 V	3.5 V to 5.5 V (mask ROM versions) 4.0 V to 5.5 V (flash memory versions)	3.0 V to 3.6 V
External bus	Address: Multiplexed/separate Data: 16-bits	Address: Multiplexed/separate Data: 16-bits	Address: Multiplexed/separate Data: 16-bits	Address: Separate/multiplexed (selectable only for CS1) Data: 8/16
Timer/counter	16-bit×2 ch 8-bit×4 ch WDT×1 ch Watch timer×1 ch	16-bit×2 ch 8-bit×6 ch WDT×1 ch Watch timer×1 ch	16-bit×10 ch WDT×1 ch Watch timer×1 ch	16-bit×7 ch WDT×1 ch
Serial interface	CSI×1 ch, CSI/UART×1 ch CSI/I²C×1 ch*, UART×1 ch	CSI×1 ch, CSI/UART×2 ch CSI/I²C×2 ch*	CSI×2 ch, CSI/UART×2 ch UART×2 ch, CSI/I²C×2 ch	CSI×1 ch, CSI/UART×1 ch UART×1 ch
A/D converter	10-bit×12 ch	10-bit×12 ch	10-bit×12 ch	10-bit×8 ch
D/A converter	-	-	-	8-bit×2 ch
DMA controller	3 ch (internal RAM-on-chip peripheral I/O)	6ch (internal RAM-on-chip peripheral I/O)	6 ch (internal RAM-on-chip peripheral I/O)	-
Other peripheral functions	-	ROM correction function	ROM correction function	Real-time output
I/O	85	83	124	65
Power consumption (mask ROM version, Typ.)	66 mW (20 MHz @ 3.3 V) 56 mW (17 MHz @ 3 V)	125 mW (20 MHz @ 5 V)	125 mW (20 MHz @ 5 V)	T.B.D.
Package	100-pin LQFP (14×14 mm) 121-pin FBGA (12×12 mm)	100-pin LQFP (14×14 mm) 100-pin QFP (14×20 mm)	144-pin LQFP (20×20 mm)	120-pin TQFP (14×14 mm) 144-pin LQFP (20×20 mm)

* : Only Y products have an on-chip I²C interface.

Product Lineup

High-End Lineup

High performance, on-chip MEMC/DMA



Features

V850E/ME2

- 215 MIPS @150 MHz, internal 1.5 V/external 3.3 V operation ROM-less microcontroller
- Large-capacity internal RAM (128 KB), real-time control
- On-chip SSCG*, EMI peak reduction
- USB full-speed (function), on-chip debugging function
  On-chip SDRAM interface
- 176-pin LQFP/240-pin FBGA

*Spread Spectrum Frequency Synthesizer Clock Generator

V850E/MA1,MA2

- 67 MIPS @50 MHz
  Internal 3.3 V/external 5 V tolerant operation single-chip microcontroller (MA1)
- ROM-less product lineup also available
- 40 MHz @3.3 V ROM-less microcontroller (MA2)
- ROM/RAM: 256 KB/10 KB (MA1), ROM-less/4 KB (MA1, MA2)
- On-chip SDRAM interface, DMA
- 144-pin LQFP/161-pin FBGA (MA1), 100-pin LQFP (MA2)

V850E/MA3

- 106 MIPS @80 MHz, internal 2.5 V/external 3.3 V operation single-chip microcontroller
- Large-capacity internal ROM/RAM (512 KB/32 KB)
- Internal single power supply flash
- SDRAM interface, motor control function, on-chip debugging function
- 144-pin LQFP/161-pin FBGA

V850E/MS1,MS2

- 47 MIPS @33 MHz, 3.3 V & 5 V single-chip microcontroller (MS1)
- ROM-less product (Max. 40 MHz) lineup available
- 33 MHz @ internal 3.3 V/external 5 V ROM-less microcontroller (MS2)
- ROM/RAM: 128 KB/4 KB (MS1), ROM-less/4 KB (MS1, MS2)
- 144-pin LQFP (MS1)/157-pin FBGA (MS1)/100-pin LQFP (MS2)

◆Product specifications◆

Item	V850E/ME2	V850E/MA3	V850E/MA1	V850E/MA2	V850E/MS1	V850E/MS2
CPU core	V850E1	V850E1	V850E1	V850E1	V850E1	V850E1
Performance	215 MIPS(@ 150 MHz)	106 MIPS(@ 80 MHz)	67 MIPS(@ 50 MHz)	-	47 MIPS(@ 33 MHz)	-
Maximum operating frequency	150 MHz	80 MHz	50 MHz	40 MHz	33 MHz (internal ROM products) 40 MHz (ROM-less products)	33 MHz
Internal flash memory	-	512 KB	256 KB	-	128 KB	-
Internal mask ROM	-	512 KB/256 KB	256 KB/128 KB/ROM-less	ROM-less	128 KB/96 KB/ROM-less	ROM-less
Internal RAM	Instruction RAM: 128 KB; Data RAM: 16 KB	32 KB/16 KB	10 KB/4 KB	4 KB	4 KB	4 KB
Cache	Instruction:8 KB	-	-	-	-	-
Power supply voltage	1.35 V to 1.65 V (internal)[Note] 3.0 V to 3.6 V (external)	2.3 V to 2.7 V (internal) 3.0 V to 3.6 V (external)	3.0 V to 3.6 V	3.0 V to 3.6 V	3.0 V to 3.6 V (internal/external) (3 V products) 3.0 V to 3.6 V (internal) (5 V products) /4.5 V to 5.5 V (external)	3.0 V to 3.6 V (internal) /4.5 V to 5.5 V (external)
Memory controller	SDRAM, SRAM, etc.	SDRAM, SRAM, etc.	SDRAM, EDO DRAM, SRAM, etc.	SDRAM, SRAM, etc.	EDO DRAM, SRAM, etc.	EDO DRAM, SRAM, etc.
External bus	Address: Separate Data: 8/16/32 bits	Address: Separate/multiplexed Data: 8/16 bits	Address: Separate Data: 8/16 bits	Address: Separate Data: 8/16 bits	Address: Separate Data: 8/16 bits	Address: Separate Data: 8/16 bits
Timer/counter	16-bit × 12 ch	16-bit× 9 ch WDT × 1 ch	16-bit × 8 ch	16-bit × 6 ch	16-bit × 8 ch	16-bit × 6 ch
Serial interface	CSI × 1 ch, CSI/UART × 1 ch UART × 1 ch	CSI/UART × 3 ch, UART/I²C × 1 ch*	CSI×1 ch, CSI/UART × 2 ch UART × 1 ch	CSI/UART × 2 ch	CSI×2 ch, CSI/UART × 2 ch	CSI/UART × 2 ch
A/D converter	10-bit × 8 ch	10-bit × 8 ch	10-bit × 8 ch	10-bit × 4 ch	10-bit × 8 ch	10-bit × 4 ch
D/A converter	-	8-bit × 2 ch	-	-	-	-
DMA controller	4 ch	4 ch	4 ch	4 ch	4 ch	4 ch
Other peripheral functions	USB×1 ch, on-chip debugging function (with trace), PWM output: 2 ch	ROM correction function On-chip debugging function	PWM output: 2 ch	-	-	-
I/O	78	112	115	79	131	57
Power consumption (mask ROM version, Typ.)	200 mW (150 MHz @ 1.5 V)	T.B.D.	528 mW (50 MHz @ 3.3 V)	416 mW (40 MHz @ 3.3 V)	330 mW (40 MHz @ 3.3 V) 272 mW (33 MHz @ 3.3 V)	218 mW (33 MHz @ 3.3 V)
Package	176-pin LQFP (24 × 24 mm) 240-pin FBGA (16 × 16 mm)	144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)	144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)	100-pin LQFP (14 × 14 mm)	144-pin LQFP (20 × 20 mm) 157-pin FBGA (14 × 14 mm)	100-pin LQFP (14 × 14 mm)

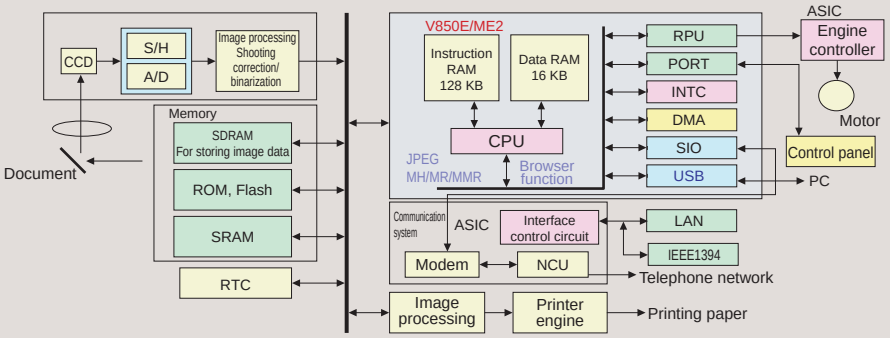
* : Only Y products have an on-chip I²C interface.

Note : 1.35 V to 1.65 V : @ 10 MHz to 133 MHz
1.40 V to 1.65 V : @ 10 MHz to 150 MHz

Application examples

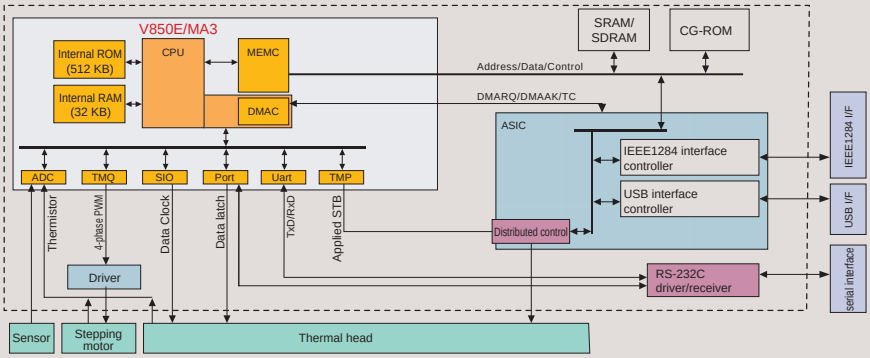
MFP (Multifunction printer)

Multi Function Printer
V850E/ME2



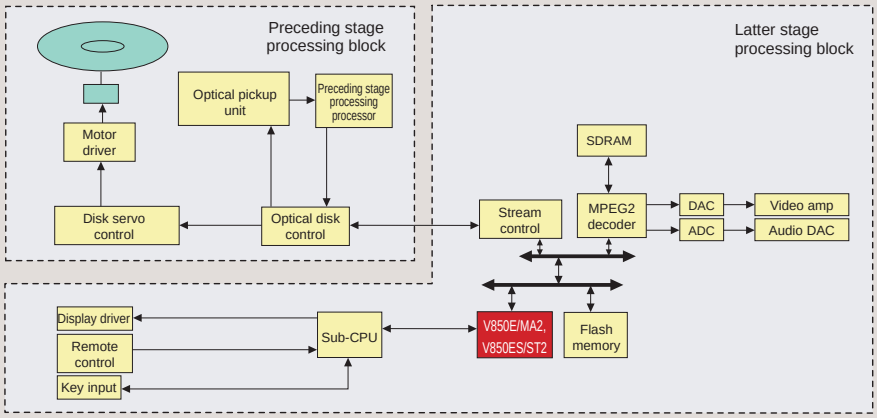
Thermal printer

Thermal Printer
V850E/MA3



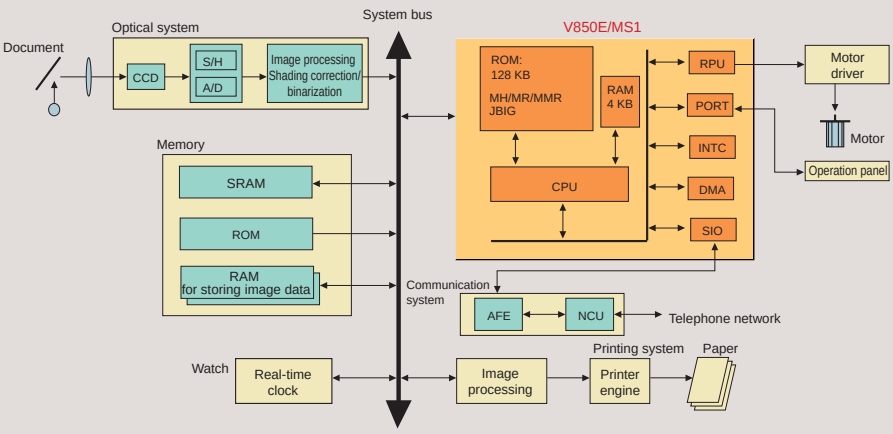
DVD player

DVD Player
V850E/MA2



Fax machine

FAX Machine
V850E/MS1

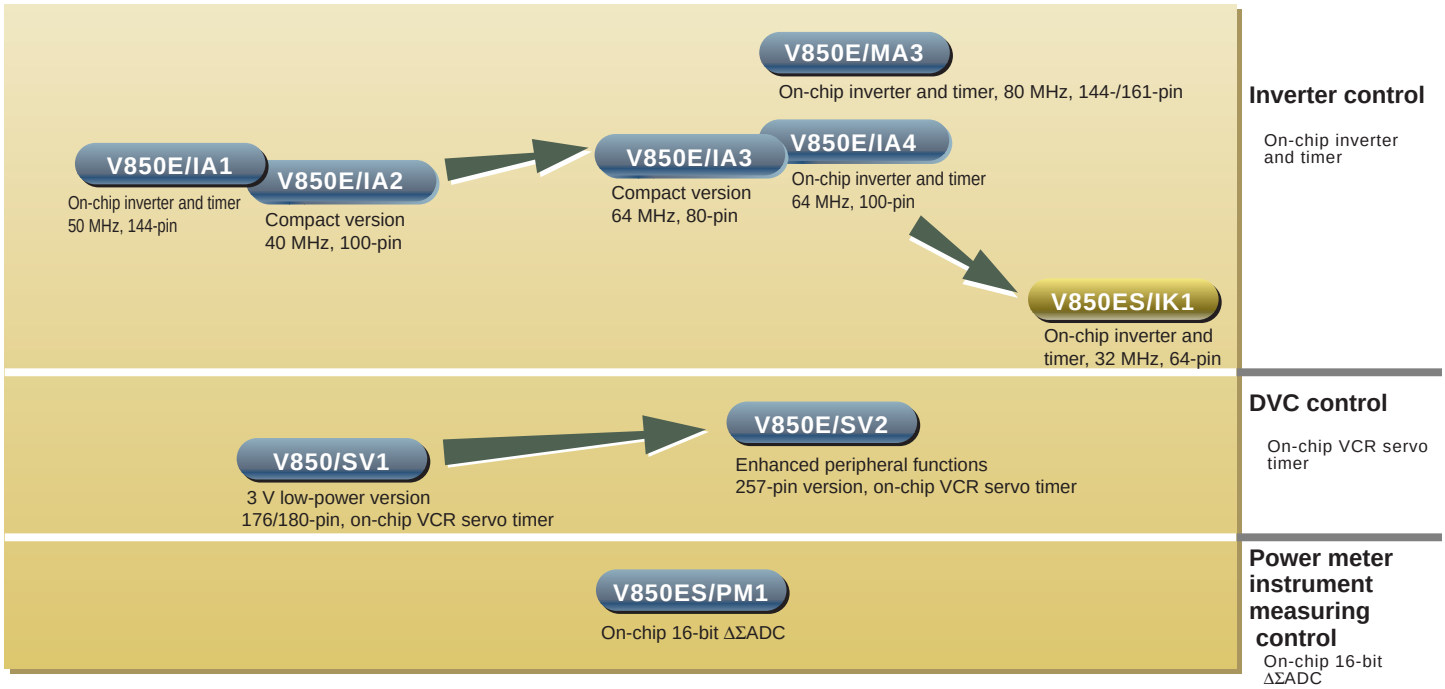


Product Lineup

ASSP Lineup (1)

Field-specific lineups

In mass production / Under development



Features

V850E/IA3, IA4

- For inverter control
- 82 MIPS @ 64 MHz, internal 2.5 V/external 5 V operation
- On-chip 6-phase sinusoidal PWM timer, on-chip operational amplifier/comparator, on-chip high-speed A/D
- On-chip debugging function (IA4 only)
- ROM/RAM: 256 KB/12 KB, 128 KB/6 KB (mask ROM version only)
- 80-pin QFP (IA3), 100-pin LQFP/100-pin QFP (IA4)

V850E/SV2

- For camcorders (incl. DVC)
- 32-bit servo timer ideal for camcorder control, boundary scan function, on-chip debugging function, and many other on-chip peripheral functions
- 55 MIPS @ 40.5 MHz, 2.5 V low-voltage/high-speed operation
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Internal single-power-supply flash
- Compact high-pin-count 257-pin FBGA (14×14 mm, 0.65 mm pitch)

V850ES/IK1

- For inverter control
- 41 MIPS @ 32 MHz, 4.5 V to 5.5 V (on-chip regulator)
- On-chip 6-phase sinusoidal PWM timer, POC/LVI, and clock monitor functions
- ROM/RAM: 128 KB/6 KB, 64 KB/4 KB
- 64-pin LQFP

V850ES/PM1

- For power meter control
- On-chip high-resolution, high-accuracy 16-bit ΔΣA/D converter
- ROM/RAM: 128 KB/10 KB, ROM-less/10 KB
- 29 MIPS @ 20 MHz, 3.0 V to 3.6 V operation
- 100-pin LQFP

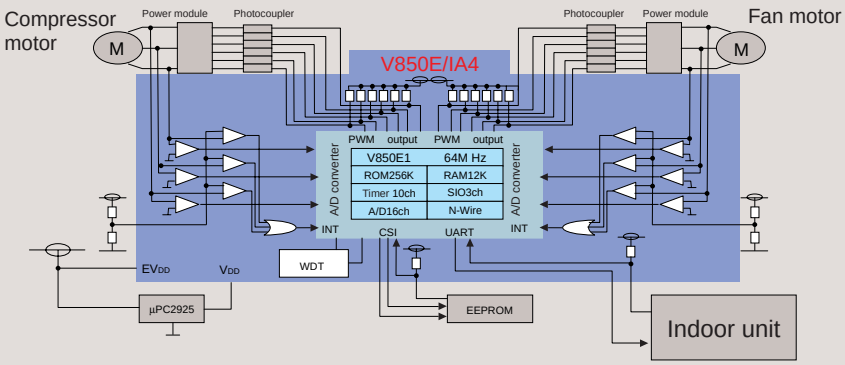
◆Product specifications◆

Item	V850E/IA1	V850E/IA2	V850E/IA3	V850E/IA4	V850ES/IK1
CPU core	V850E1	V850E1	V850E1	V850E1	V850ES
Performance	67 MIPS (@ 50 MHz)	54 MIPS (@ 40 MHz)	82 MIPS (@ 64 MHz)	82 MIPS (@ 64 MHz)	41 MIPS (@ 32 MHz)
Maximum operating frequency	50 MHz	40 MHz	64 MHz	64 MHz	32 MHz
Internal flash memory	256 KB	128 KB	256 KB	256 KB	128 KB
Internal mask ROM	256 KB	128 KB	128 KB	256 KB/128 KB	128 KB/64 KB
Internal RAM	10 KB	6 KB	12 KB/6 KB	12 KB/6 KB	6 KB/4 KB
Power supply voltage	3.0 V to 3.6 V (internal) 4.5 V to 5.5 V (external)	4.5 V to 5.5 V	2.3 V to 2.7 V (internal) 4.5 V to 5.5 V (external)	2.3 V to 2.7 V (internal) 4.5 V to 5.5 V (external)	3.5 V to 5.5 V
External bus	Address: Multiplexed Data: 8/16 bits	Address: Multiplexed Data: 8/16 bits	-	-	-
Timer/counter	16-bit × 8 ch	16-bit × 7 ch	16-bi t × 8 ch WDT × 1 ch	16-bit × 9 ch WDT × 1 ch	16-bit × 7 ch WDT × 1 ch
Serial interface	CSI × 2ch, UART × 3ch	CSI × 1 ch, CSI/UART × 1 ch UART × 1 ch	CSI × 1 ch, CSI/UART × 1 ch UART × 1 ch	CSI × 1 ch, CSI/UART × 1 ch UART × 1 ch	CSI × 1 ch, UART × 2 ch
A/D converter	10-bit × (8 ch + 8 ch)	10-bit × (6 ch + 8 ch)	10-bit×(4 ch + 2 ch), 8/10-bit×6 ch	10-bit× (4 ch + 4 ch), 8/10-bi t× 8 ch	10-bit × (4 ch+4 ch)
D/A converter	-	-	-	-	-
DMA controller	4 ch	4 ch	4 ch	4 ch	-
Other peripheral functions	FCAN × 1 ch	-	ROM correction function operational amplifier, comparator, pull-up function	On-chip debugging and ROM correction functions Operational amplifier, comparator, pull-up function	ROM correction function, pull-up function, POC/LVI, clock monitor function
I/O	83	53	50	64	39
Power consumption (mask ROM version, Typ.)	630 mW (50 MHz @ 3.3 V)	440 mW (40 MHz @ 5 V)	175 mW (64 MHz @ 2.5 V)	175 mW (64 MHz @ 2.5 V)	T.B.D.
Package	144-pin LQFP (20 × 20 mm)	100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)	80-pin QFP (14 × 14 mm)	100-pin QFP (14 × 20 mm) 100-pin LQFP (14 × 14 mm)	64-pin LQFP (14 × 14 mm)

Application examples

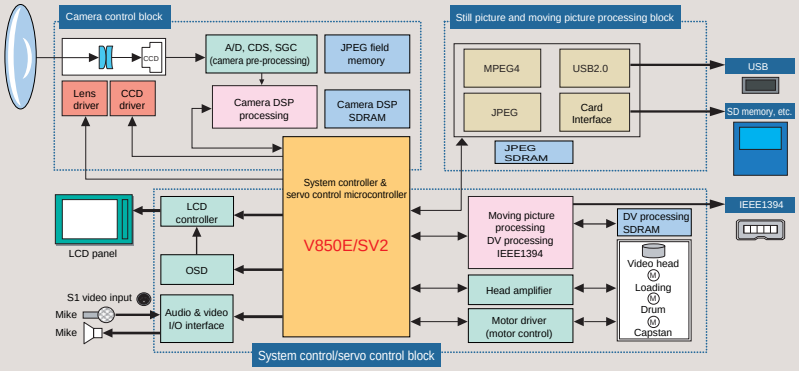
■ Air conditioner

Air Conditioner
V850E/IA4



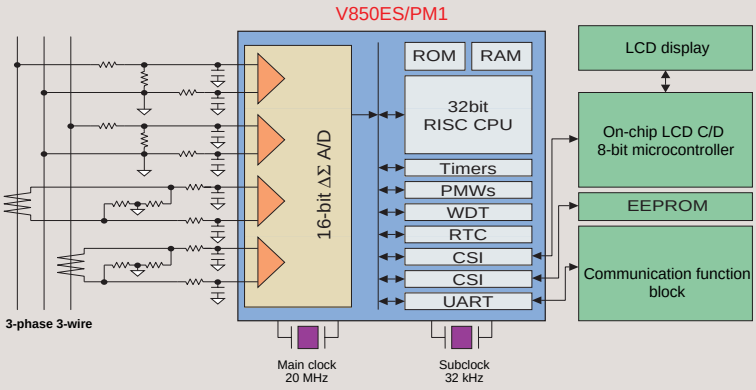
■ DVC

Digital Video Camera
V850E/SV2



■ Power meter

Power Meter
V850ES/PM1



Item	V850/SV1	V850E/SV2	V850ES/PM1
CPU core	V850	V850E1	V850ES
Performance	23 MIPS (@ 20 MHz)	55 MIPS (@ 40.5 MHz)	29 MIPS (@20 MHz)
Maximum operating frequency	20 MHz	40.5 MHz	20 MHz
Internal flash memory	384 KB/256 KB	512 KB	-
Internal mask ROM	384 KB/256 KB/192 KB	512 KB	128 KB/ROM-less
Internal RAM	16 KB/8 KB	24 KB	10 KB
Power supply voltage	3.1 V to 3.6 V @ 20 MHz 2.7 V to 3.6 V @ 16 MHz	2.3 V to 2.7 V (internal) 2.7 V to 3.6 V (external)	3.0 V to 3.6 V @ 20 MHz, 2.7 V to 3.6 V @ 10 MHz, 2.2 to 3.6 V @ 32.768 kHz
External bus	Address: Multiplexed Data: 16 bits	Address: Multiplexed/separate Data: 8/16 bits	Address : Separate Data : 8/16 bits
Timer/counter	24-bit × 2 ch, 16-bit × 2 ch 8-bit×8ch, WDT × 1 ch, watch timer × 1 ch	32-bit × 1 ch, 16-bit × 12 ch 8-bit × 12 ch, WDT × 1 ch	16-bit × 6 ch, 8-bit × 2 ch WDT × 1 ch
Serial interface	CSI × 1 ch, CSI/UART × 2 ch CSI/I²C × 2 ch*	CSI × 5 ch, CSI/UART × 1 ch, UART×1 ch, I²C × 1 ch*	CSI × 2 ch, UART × 2 ch
A/D converter	10-bit × 16 ch	10-bit × 24 ch	16-bit ΔΣ × 6 ch
D/A converter	-	-	-
DMA controller	6 ch (internal RAM-on-chip peripheral I/O)	4 ch	-
Other peripheral functions	ROM correction function, dedicated PWM output × 4, Hsync/Vsync separation circuit	On-chip debugging function, boundary scan function ROM correction function, dedicated PWM output: 5 ch	ROM correction function, dedicated PWM output: 4 ch Real-time counter (watch function)
I/O	151	195	80
Power consumption (mask ROM version, Typ.)	82 mW (20 MHz @3.3 V)	134 mW (40.5 MHz @ 2.5 V)	81 mW (20 MHz @3.3 V)
Package	176-pin LQFP (24 × 24 mm) 180-pin FBGA (13 × 13 mm)	257-pin FBGA (14 × 14 mm)	100-pin LQFP (14 × 14 mm)

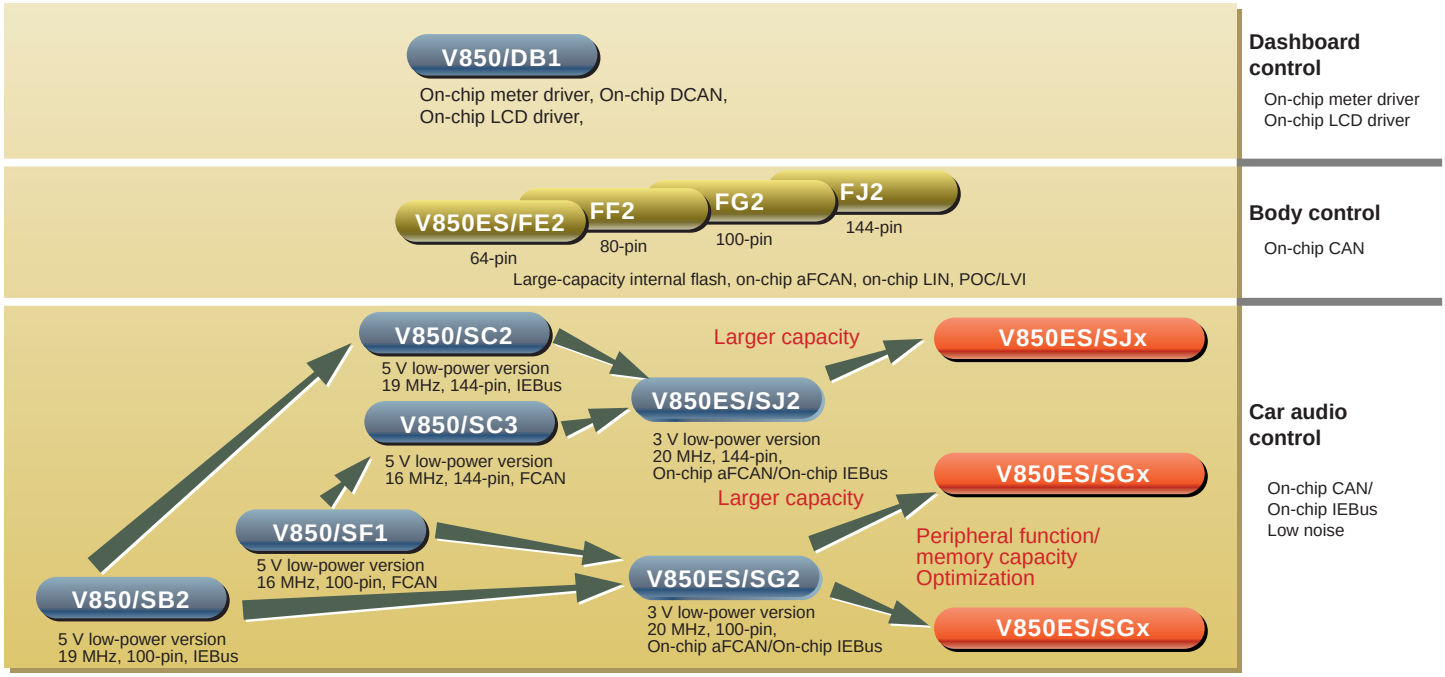
* : Only Y products have an on-chip I²C interface.

Product Lineup

ASSP Lineup (2)

Field-specific lineups

In mass production | Under development | Under planning



Features

V850/DB1

- For automotive electronics (body control applications)
- ROM/RAM : 128 KB/6 KB
- On-chip DCAN controller (2 ch max.)
- 18 MIPS @ 16 MHz, 4.0 to 5.5 V operation
- 128-pin QFP

V850ES/SG2, SJ2

- For car audio
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM : 640 KB/48 KB, 512 KB/40 KB, 384 KB/32 KB, 256 KB/24 KB (SG2 only)
- On-chip IEBus controller (1 ch), on-chip aFCAN controller (2 ch max.)
- 29 MIPS @ 20 MHz, 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip debugging function
- 100-pin LQFP/100-pin QFP (SG2), 144-pin LQFP (SJ2)

V850ES/FE2, FF2, FG2, FJ2

- For automotive electronics (body control applications)
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 512 KB/20 KB, 384 KB/16 KB, 256 KB/12 KB, 128 KB/6 KB
- On-chip aFCAN controller (4 ch max.), LIN function compatible UART, POC/LVI
- 29 MIPS @ 20 MHz, 4.0 to 5.5 V operation
- 64-pin TQFP (FE2)/80-pin TQFP (FF2)/100-pin LQFP (FG2)/144-pin LQFP (FJ2)

V850/SF1

- For car audio
- Low EMI noise
- On-chip FCAN controller (2 ch max.)
- ROM/RAM: 256 KB/16 KB, 128 KB/12 KB
- 100-pin LQFP/100-pin QFP

◆Product specifications◆

Item	V850ES/Fx2				
	FE2	FF2	FG2	FJ2	
CPU core	V850ES				
Performance	29 MIPS (@ 20 MHz)				
Maximum operating frequency	20 MHz				
Internal flash memory	128 KB/64 KB	256 KB/128 KB	384 KB/256 KB/128 KB	384 KB/256 KB	512 KB
Internal mask ROM	128 KB/64 KB	256 KB/128 KB	256 KB/128 KB	-	-
Internal RAM	6 KB/4 KB	12 KB/6 KB	16 KB/12 KB/6 KB	16 KB/12 KB	20 KB
Power supply voltage	4.0 V to 5.5 V				
External bus	-				Address: Multiplexed bus Data: 8/16 bits
Timer/counter	16-bit × 6 ch WDT × 1 ch, watch timer × 1 ch		16-bit × 7 ch WDT × 1 ch, watch timer × 1 ch	16-bit × 8 ch WDT × 1 ch, watch timer × 1 ch	
Serial interface	CSI × 2 ch, LIN-compatible UART × 2 ch		CSI × 2 ch, LIN-compatible UART × 3 ch	CSI × 3 ch, LIN-compatible UART × 3 ch	CSI × 3 ch, LIN-compatible UART × 4 ch
A/D converter	10-bit × 10 ch	10-bit × 12 ch	10-bit × 16 ch	10 bit × 24 ch	
D/A converter	-				
DMA controller	-		4 ch		
Other peripheral functions	POC/LVI function, clock monitor function, RAM hold flag				
	aFCAN × 1 ch		aFCAN × 2 ch		aFCAN × 4 ch
I/O	51	67	84	128	
Power consumption (mask ROM version, Typ.)	155 mW (20 MHz @ 5 V)			200 mW (20 MHz @ 5 V)	-
Package	64-pin TQFP (10 × 10 mm)	80-pin TQFP (12×12 mm)	100-pin LQFP (14 ×14 mm)	144-pin LQFP (20 × 20 mm)	

V850/SB2

- Low EMI noise
- Large-capacity memory and large memory selection
- ROM/RAM:512K/24KB, 384KB/24KB, 256KB/16KB, 128KB/8KB
- On-chip IEBus controller (1 ch)
- 100-pin QFP/100-pin LQFP

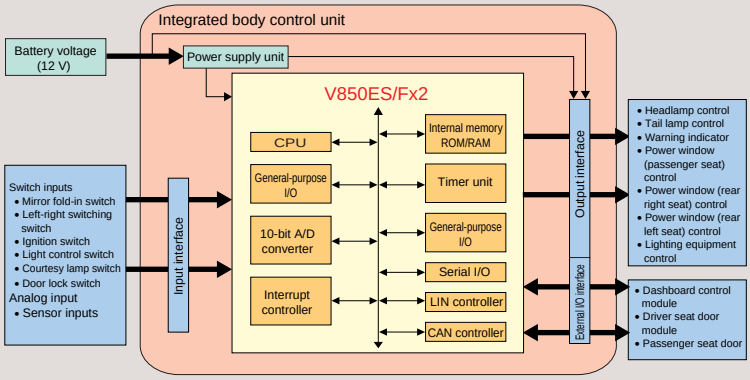
V850/SC2,SC3

- Low EMI noise
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Enhanced peripheral functions for SB1
- On-chip IEBus controller (V850/SC2 : 1 ch) ,
  On-chip FCAN controller (V850/SC3 : 2 ch max.)
- 144-pin LQFP

Application examples

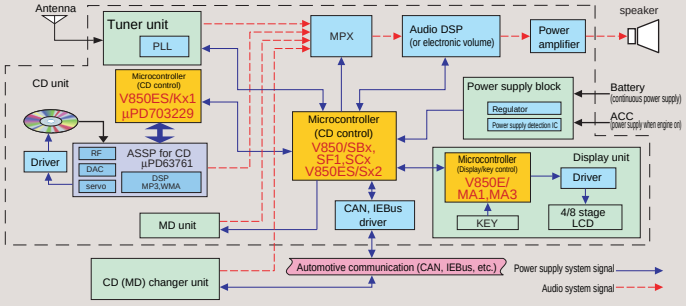
Dashboard

Dashboard
V850ES/Fx2



Car audio

Car Audio
V850/SF1

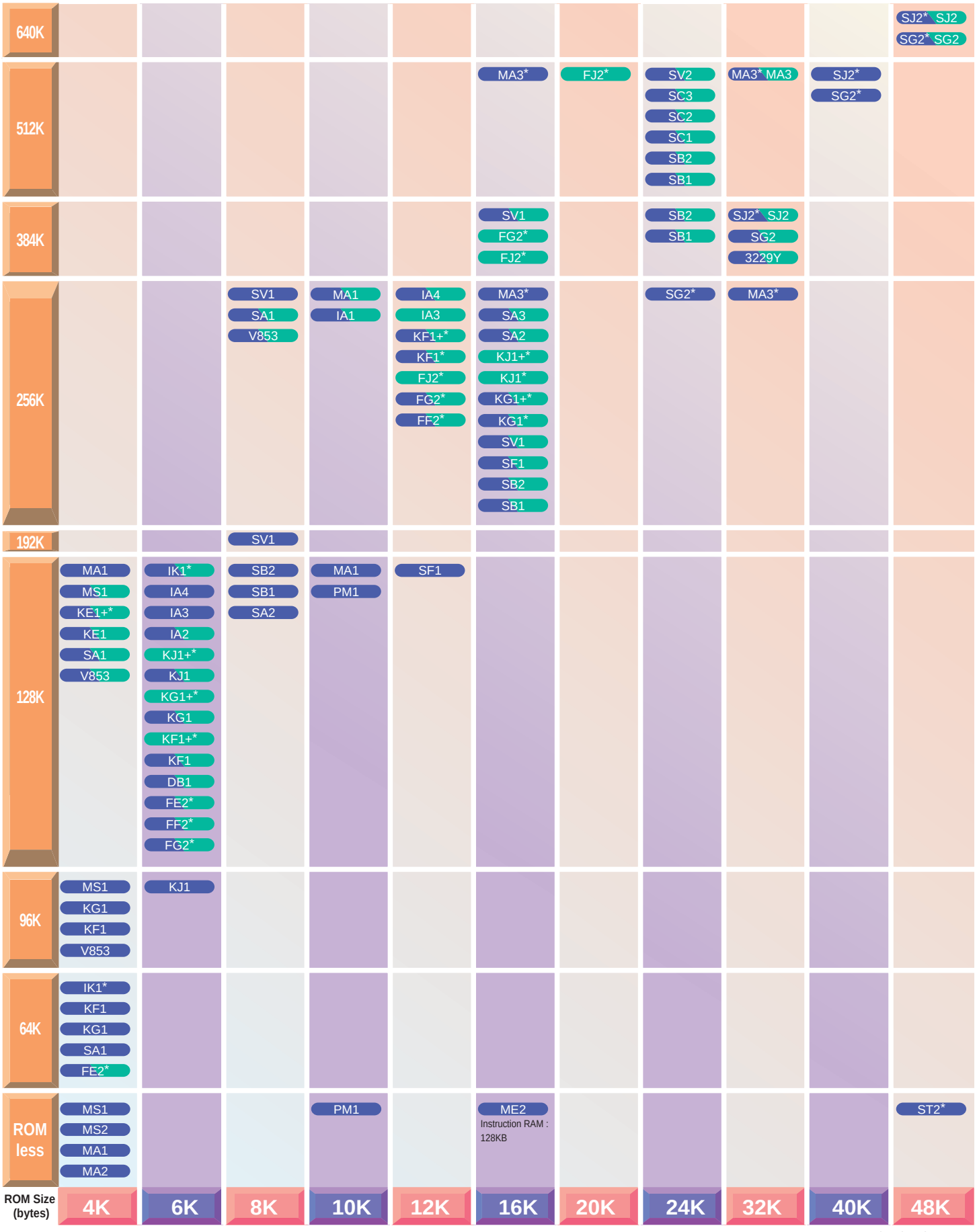


Item	V850/SB2	V850/SCx		V850/SF1	V850/DB1
		SC2	SC3		
CPU core	V850	V850		V850	V850
Performance	22 MIPS (@ 19 MHz)	21 MIPS (@ 19 MHz)	18MIPS (@ 16 MHz)	18 MIPS (@ 16 MHz)	18 MIPS (@ 16MHz)
Maximum operating frequency	19 MHz/13 MHz (main clock) 32.768 kHz (subclock)	19 MHz (main clock) 32.768 kHz (subclock)	16 MHz (main clock) 32.768 kHz (subclock)	16 MHz	16 MHz
Internal flash memory	512 KB/384 KB/256 KB	512 KB		256 KB	128 KB
Internal mask ROM	512 KB/384 KB/256 KB/128 KB	512 KB		256 KB/128 KB	128 KB
Internal RAM	24 KB/16 KB/8 KB	24 KB		16 KB/12 KB	6 KB
Power supply voltage	4.0 V to 5.5 V	3.5 V to 5.5 V (mask version) 4.0 V to 5.5 V (flash version)		3.5 V to 5.5 V (mask version), 4.0 V to 5.5 V (flash version) 3.5 V to 5.5 V @ 32.768 kHz	4.0 V to 5.5 V
External bus	Address: Multiplexed/separate Data: 16-bits	Address: Multiplexed/separate Data: 16-bits	Address: Multiplexed Data: 16-bit	Address: Multiplexed Data: 16-bit	-
Timer/counter	16-bit × 2 ch, 8-bit × 6 ch WDT × 1 ch, watch timer × 1 ch	16-bit × 10ch WDT × 1 ch, watch timer × 1 ch		16-bit × 8ch WDT × 1ch, watch timer × 1 ch	16-bit × 3 ch, 8-bit × 2 ch WDT × 1 ch, watch timer × 1 ch
Serial interface	CSI × 1 ch, CSI/UART × 2 ch CSI/I²C × 2 ch	CSI × 2 ch, CSI/UART × 2 ch UART × 2 ch, CSI/I²C × 2 ch		CSI × 1 ch, CSI/UART × 2 ch CSI/I²C × 1 ch	CSI × 3 ch, UART × 2 ch
A/D converter	10-bit × 12 ch	10-bit × 12 ch		10-bit × 12 ch	10-bit × 8 ch
D/A converter	-	-		-	-
DMA controller	6 ch (internal RAM-on-chip peripheral I/O)	6 ch (internal RAM-on-chip peripheral I/O)		6 ch (internal RAM-on-chip peripheral I/O)	-
Other peripheral functions	IEBus × 1 ch ROM correction function	IEBus × 1 ch ROM correction function	FCAN × 2 ch ROM correction function	FCAN × 2 ch, ROM correction function	meter controlPWM (8-bit) × 24 ch DCAN × 2 ch (flash version)/1 ch (mask version)
I/O	83	124		84	107
Power consumption (mask ROM version, Typ.)	125 mW (19 MHz @ 5 V)	120 mW (19 MHz @ 5V)	110 mW (16 MHz @ 5 V)	75 mW (16 MHz @ 5 V)	120mW (16 MHz @ 5V)
Package	100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)	144-pin LQFP (20 × 20 mm)		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)	128-pin QFP (20 × 20 mm)

Product Lineup

Memory Lineup

Flash memory version　Mask ROM version　Mask ROM/flash memory version



* : Under development

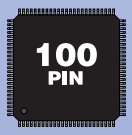
Package Lineup

No. of pins	121 pins
Type	FBGA (F1)
Size	12×12 mm
Pitch	0.8 mm
Thickness	1.13 mm
Mounted products	SA1, SA3

No. of pins	64 pins
Type	LQFP (GB)
Size	10×10 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	KE1, KE1+

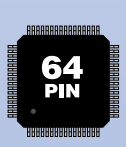
No. of pins	161 pins
Type	FBGA (F1)
Size	13×13 mm
Pitch	0.8 mm
Thickness	1.13 mm
Mounted products	MA1, MA3

No. of pins	64 pins
Type	TQFP (GB)
Size	10×10 mm
Pitch	0.5 mm
Thickness	1.0 mm
Mounted products	FE2



No. of pins	100 pins
Type	LQFP (GC)
Size	14×14 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	KG1, KG1+, SA1, SB1, SB2, SF1, SG2, PM1, FG2, MS2, MA2, IA2, IA4, V853, µPD70F3229Y, 703229Y

No. of pins	180 pins
Type	FBGA (F1)
Size	13×13 mm
Pitch	0.8 mm
Thickness	1.13 mm
Mounted products	SV1

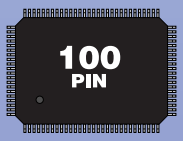


No. of pins	64 pins
Type	TQFP (GK)
Size	12×12 mm
Pitch	0.65 mm
Thickness	1.0 mm
Mounted products	KE1, KE1+

No. of pins	120 pins
Type	TQFP (GC)
Size	14×14 mm
Pitch	0.4 mm
Thickness	1.0 mm
Mounted products	ST2

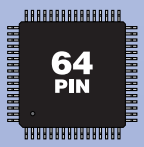
No. of pins	157 pins
Type	FBGA (F1)
Size	14×14 mm
Pitch	0.8 mm
Thickness	0.96 mm
Mounted products	MS1

No. of pins	80 pins
Type	TQFP (GK)
Size	12×12 mm
Pitch	0.5 mm
Thickness	1.0 mm
Mounted products	KF1, KF1+, FF2

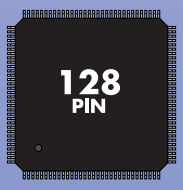


No. of pins	100 pins
Type	QFP (GF)
Size	14×20 mm
Pitch	0.65 mm
Thickness	1.4 mm
Mounted products	KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4

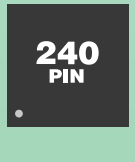
No. of pins	257 pins
Type	FBGA (F1)
Size	14×14 mm
Pitch	0.65 mm
Thickness	1.13 mm
Mounted products	SV2



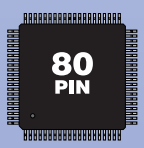
No. of pins	64 pins
Type	LQFP (GC)
Size	14×14 mm
Pitch	0.8 mm
Thickness	1.4 mm
Mounted products	IK1



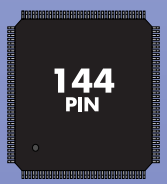
No. of pins	128 pins
Type	QFP (GJ)
Size	20×20 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	DB1



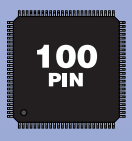
No. of pins	240 pins
Type	FBGA (F1)
Size	16×16 mm
Pitch	0.8 mm
Thickness	1.13 mm
Mounted products	ME2



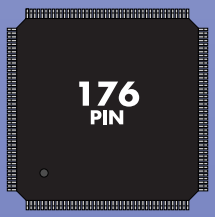
No. of pins	80 pins
Type	QFP (GC)
Size	14×14 mm
Pitch	0.65 mm
Thickness	1.4 mm
Mounted products	KF1, KF1+, IA3



No. of pins	144 pins
Type	LQFP (GJ)
Size	20×20 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	KJ1, KJ1+, SC1, SC2, SC3, SJ2, ST2, FJ2, MS1, MA1, MA3, IA1



No. of pins	100 pins
Type	TQFP (GC)
Size	14×14 mm
Pitch	0.5 mm
Thickness	1.0 mm
Mounted products	SA2

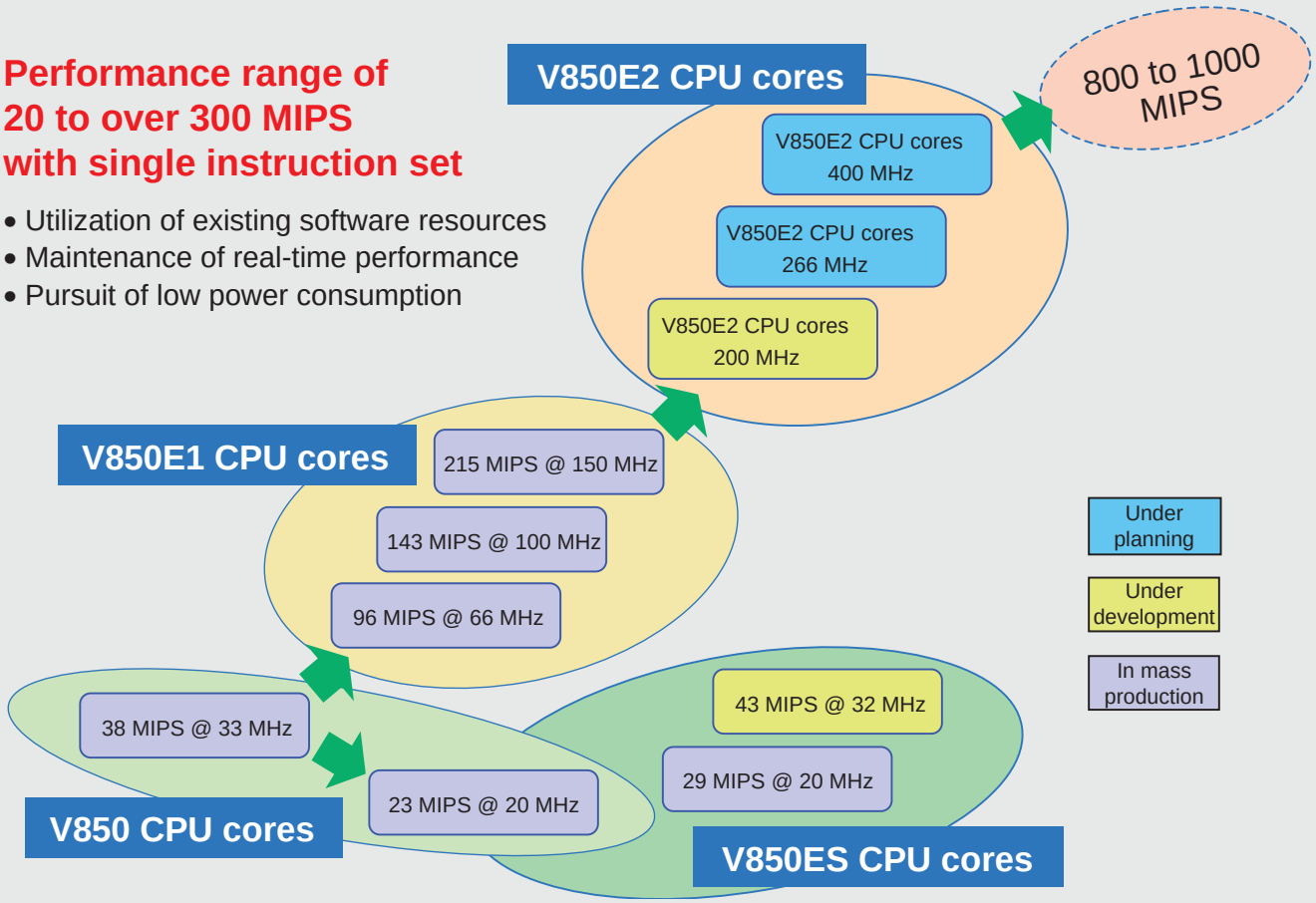


No. of pins	176 pins
Type	LQFP (GM)
Size	24×24 mm
Pitch	0.5 mm
Thickness	1.4 mm
Mounted products	SV1, ME2

CPU Roadmap

Performance range of 20 to over 300 MIPS with single instruction set

- Utilization of existing software resources
- Maintenance of real-time performance
- Pursuit of low power consumption



CPU Core Function Comparison

CPU Core / Function	V850	V850ES	V850E1	V850E2
Maximum operating frequency	20/33 MHz	20/32 MHz	66⇒100⇒150 MHz	200⇒266⇒400 MHz
Instructions	47	80	80	89
Maximum program memory space	16 MB	16 MB	64 MB	512 MB (internal 128 MB)
Maximum data memory space	16 MB	16 MB	256 MB	4 GB
Higher performance	5-stage pipeline Harvard architecture	Improved pipeline • Non-blocking load/store instructions - Parallel instruction execution (instruction execution in internal ROM) • Addition of branching/load pipe • Shift to 3-operand manipulations in 1 slot		• 7-stage pipeline Simultaneous execution of 2 instructions with 3 pipelines that can operate independently from each other
High code efficiency	2-byte instructions CISC instructions	Addition of C language compatible instructions (Switch instruction, Callt instruction, data conversion instruction, Prepare/Dispose instruction)		32-bit relative branch instruction 3-operand instruction Sum-of-products instruction Bit search instruction
Multiplier	16×16 bits⇒32 bit multiplication	16×16 bits ⇒32-bit operation 32×32 bits⇒64-bit operation (32-bit multiply instruction support)	16×16 bits⇒32-bit operation 32×32 bits⇒64-bit operation	
Interrupt responsiveness	11 to 18 clocks	4 to 10 clocks		

System LSI Support

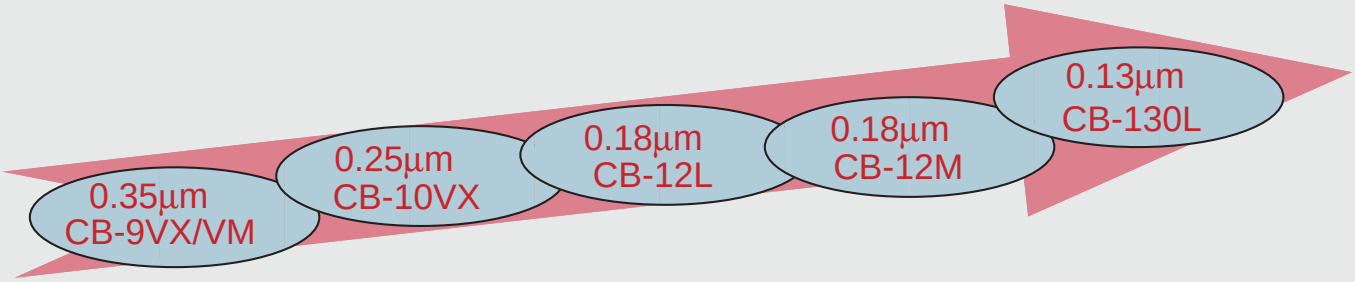
◆**Use of same development methods for standard V850 Series products, ASIC microcontrollers**

- Quick market introduction of standard products
- System optimization through shift to system LSIs

◆**CPU core development considering system LSIs**

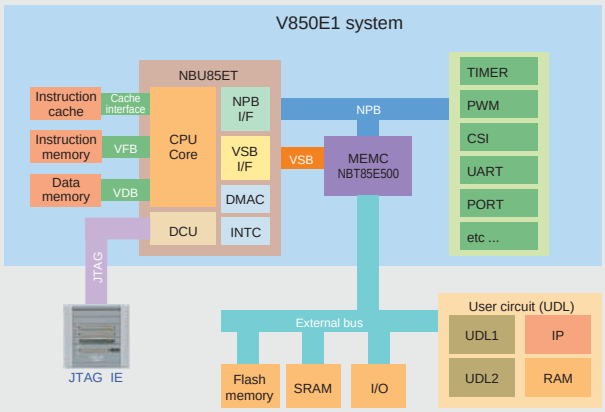
- Release of cores that support on-chip debugging
- 2-stage structure consisting of 32-bit sync system bus & 16-bit async peripheral function bus
- Large choice of peripheral function macros

◆**Many supported processes and large range of required performance, and power consumption**



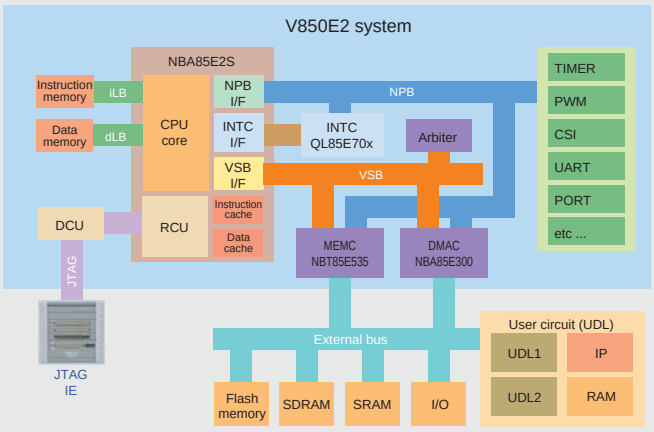
V850E1 system configuration example

NPB: Peripheral I/O bus
VSB: System bus
VFB: Internal instruction bus
VDB: Internal data bus



V850E2 system configuration example

NPB: Peripheral I/O bus
VSB: System bus
iLB: Internal instruction bus
dLB: Internal data bus



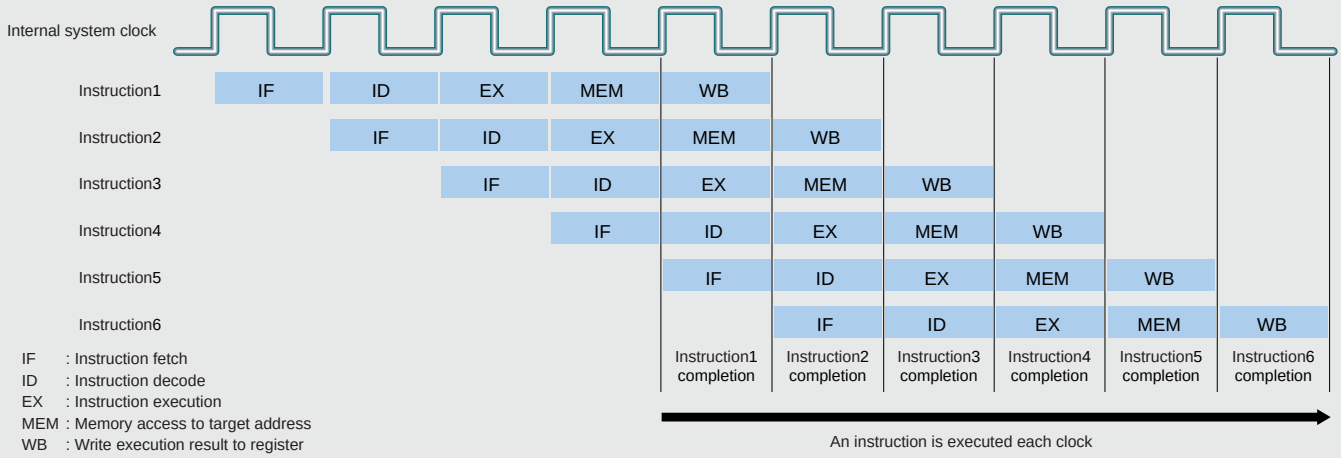
V850 Series Common Architecture

The V850 Series, which consists of single-chip RISC microcontrollers that use an architecture optimized for embedding, has the following features.

- 5-stage pipeline processing
- Harvard architecture
- 32 general-purpose registers
- Simple addressing
- 2-byte basic instruction set
- Support of CISC-like instructions
- Multi-status flags
- DSP function
- 32-bit barrel shifter

5-stage pipeline processing

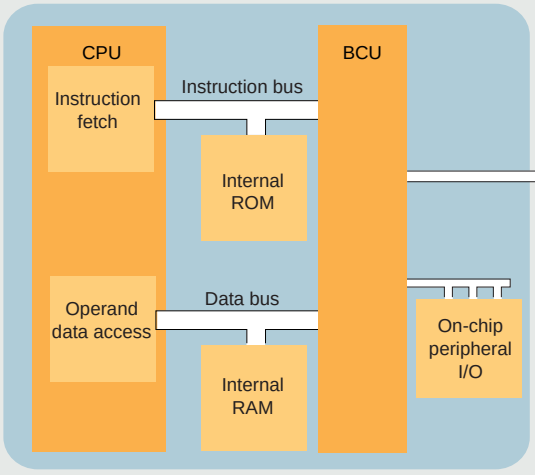
The V850 Series uses a 5-stage pipeline structure (5 stages from instruction fetch to writeback) that supports simultaneous processing of 5 instructions, thus enabling the execution of almost all instructions in just one clock.



IF : Instruction fetch
ID : Instruction decode
EX : Instruction execution
MEM : Memory access to target address
WB : Write execution result to register

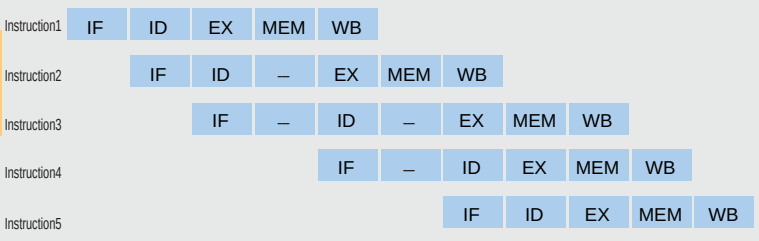
Harvard architecture

The V850 Series uses the Harvard architecture, which is designed so that the instruction bus and data bus can operate completely independently from each other, thereby preventing pipeline operation problems and ensuring efficient instruction execution.



In the case of an architecture other than the Harvard architecture, the MEM stage of instruction 1 and the IF stage of instruction 4, and the MEM stage of instruction 2 and the IF stage of instruction 5 conflict, causing bus waits. This in turn causes the pipeline operation to become disordered and lowers the instruction execution speed.

Pipeline Operation of Non-Harvard Architecture

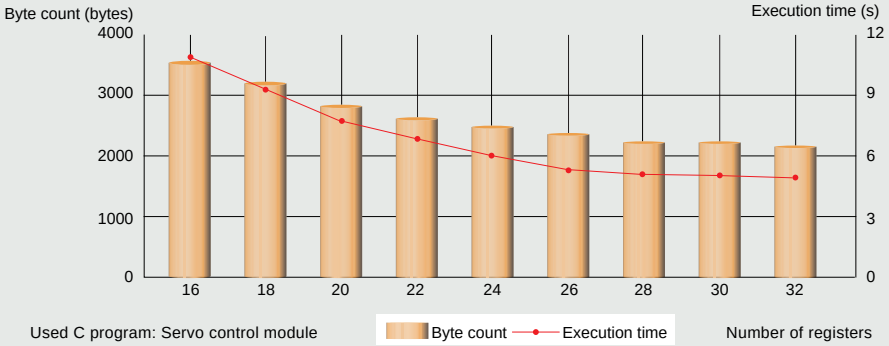


–:Idles inserted due to bus wait

32 general-purpose registers

The V850 Series provides 32 general-purpose registers. Along with a hardware environment that is ideal for program execution, the development environment, including compilers, exploits these 32 registers to achieve program generation with superior code efficiency and execution performance.

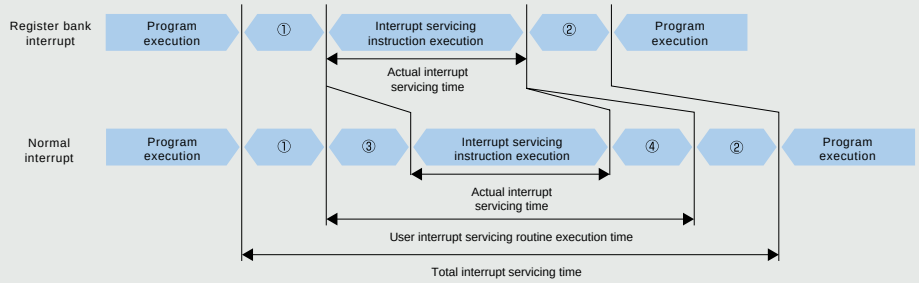
Comparison of Performance/Object Efficiency According to Number of Registers



For example, looking at the program execution time and code size changes when the number of registers used by the compiler is changed using the servo control module, we can see that the larger the number of registers, the better the program execution speed and the smaller the code size. However, from about 26 registers, the improvement in terms of execution speed and code size becomes smaller, and in the neighborhood of 32 registers, there are no more changes. This is why the V850 Series has been provided with 32 registers as the strict minimum requirement.

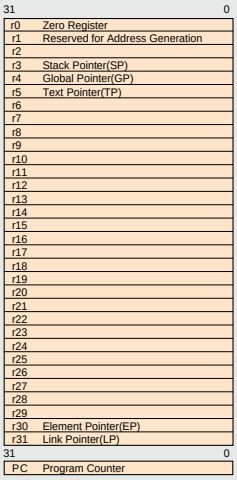
Software register bank

The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.



① Save the program counter, etc., to a save register.
② Execute the interrupt restore instruction. Restore the program counter value, etc., from the save register.
③ Save general-purpose registers to stacks.
④ Restore general-purpose registers from stacks.

General-purpose register configuration



Name	Application	Operation
r0	Zero register	Always holds "0"
r1	Assembler reservation	Used as working register for address generation
r2	Address/data variable register (If real-time OS being used does not use r2)	
r3	Stack pointer	Used for stack frame generation during function call
r4	Global pointer	Used when accessing global variables in the data area
r5	Text pointer	Used as register for specifying the beginning of the text area (program code allocation)
r6-r29	Address/data variable register	
r30	Element pointer	Used as base pointer for address generation during memory access
r31	Link pointer	Used during function call by compiler
PC	Program counter	Holds instruction addresses during program execution

System register configuration

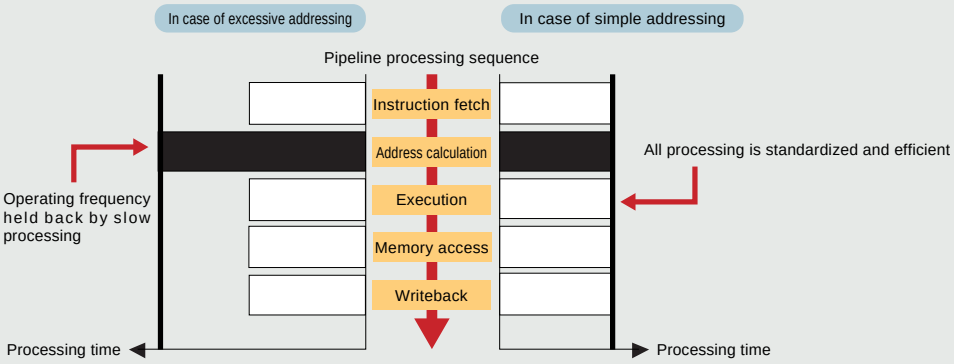
	No.	System Register Name	Operand Specification		Application
			LDSR	STSR	
	0	EIPC	○	○	Register for saving status during interrupt
	1	EIPSW	○	○	
	2	FEPC	○	○	Register for saving status during NMI
	3	FEPSW	○	○	
	4	ECR	×	○	Interrupt source register
	5	PSW	○	○	Program status word
Supported by other than V850 CPU core products	16	CTPC	○	○	Register for saving status during CALLT execution
	17	CTPSW	○	○	
	18	DBPC	○	○	Register for saving status during exception/debug trap
	19	DBPSW	○	○	
	20	CTBP	○	○	CALLT base pointer
	6-15, 21-31	Reserved	×	×	

× : Access prohibited
○ : Access enabled
LDSR: Instruction to load general-purpose register contents to system register
STSR: Instruction to store system register contents to general-purpose register

Simple addressing

The increased amount of address calculations in the CPU in the case of complex addressing causes disturbances in the pipeline operation. As a result, address calculation becomes a bottleneck for pipeline processing and raising the frequency to increase the performance becomes difficult. The V850 Series avoids this problem by supporting only simple addressing.

Pipeline Processing Time and CPU Operating Frequency

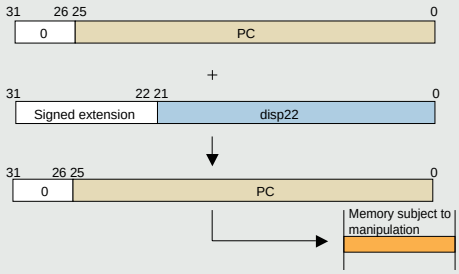


Addressing mode

●Instruction addresses

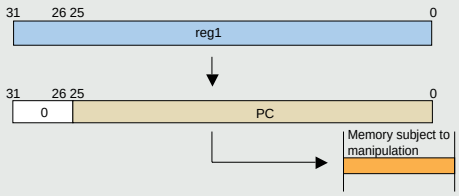
•Relative addressing (PC dependent)

Add 9 signed bits or 22 signed bits of data of the instruction code to the program counter.



•Register addressing (register indirect)

Transfer the contents of the general-purpose register specified by the instruction (reg1) to the program counter (PC).



●Operand addresses

•Register addressing

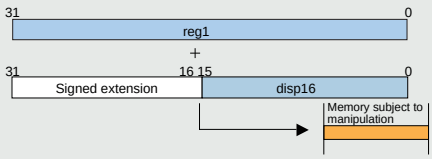
Addressing that accesses the general-purpose register specified by the general-purpose specification field or a system register as an operand.

•Immediate addressing

Addressing of 5-bit data or 16-bit data for manipulation in the instruction code.

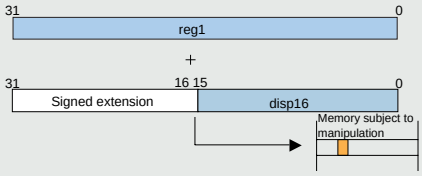
•Based addressing

Addressing that accesses memory, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) as the operand address.



•Bit addressing

Addressing that accesses 1 bit of 1 byte of the memory space, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) that has been sign extended to word length as the operand address.



2-byte basic instruction set

The V850 Series employs a 2-byte instruction code to perform basic processing to enable compact program development equivalent to 16-bit CISC microcontrollers.

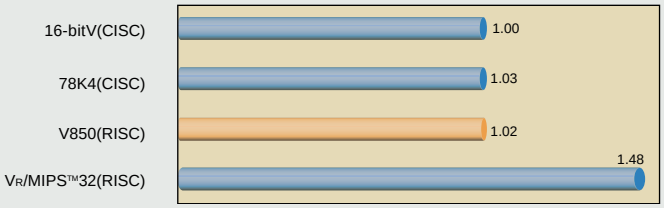
•Improved object efficiency through ROMization programming

Application of 2-byte instructions to all basic processing, consisting of load, store, arithmetic/logic operations, and branching.

•To realize ease of use, restrictions on 16-bit fixed-length instructions are partially removed through incorporation of 32-bit instructions.

•Bit manipulation instructions, etc.

Object Code Size Comparison
(Dhrystone 1.1/Large model)



CISC-like instructions for embedding (bit manipulation instructions)

The V850 Series supports bit manipulation instructions suitable for flag manipulation on I/O registers, which play a large role in embedding control.

- Improvement of operability of memory mapped I/Os for control purposes
- Manipulation of any 1 bit of byte data in the memory space
- Provision of test (tst1)/set (set1)/clear (clr1)/invert (not1)
- Effective for reducing object size and execution time since flags can be manipulated in 1-bit units with 1 instruction

Example: Setting (1) bit 6 of ASIM00 register

Item \ Bit Manipulation Instruction	When Used	When Not Used	
Coding example	set1 6, ASIM00[r0]	ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0]	add -4, sp st.w r20, 0[sp]] Save r20 ld.b ASIM00[r0], r20 ori 0x0040, r20, r20 st.b r20, ASIM00[r0] ld.w 0[sp], r20 add 4, sp] Restore r20
Object size	4 bytes	12 bytes	24 bytes
Execution time	4 clocks	4 clocks	8 clocks

Multi-status flags

In the V850 Series, calculation results are reflected in registers as status flags. As a result, delay branching such as can be seen in the RISC microcontrollers of other manufacturers does not occur and programs can be coded with the same feel as CISC microcontrollers.

- Easy recording with assembler
- Improved object efficiency and execution speed

ZERO : Zero processing
PLUS : Positive processing
MINUS : Negative processing

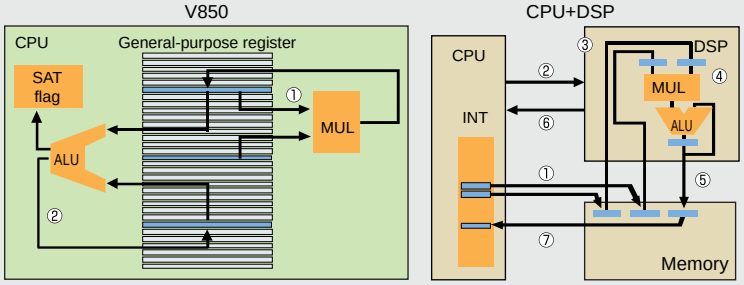
Example: Program that branches to positive/negative/zero according to register contents

CISC Microcontroller	V850	Other Manufacturer's RISC Microcontroller
cmp ax, 0 jz ZERO jgt PLUS jmp MINUS	cmp 0, r10 bz ZERO bgt PLUS br MINUS	cmp/eq #0, r10 bt ZERO cmp/pl r10 bt PLUS bra MINUS nop ;For delay branching

DSP function

The V850 Series provides a DSP function for executing high-speed calculations and product-sum operations indispensable for digital signal processing such as image and speech processing.

- Direct data handling via general-purpose registers
- Realization of digital signal processing through general-purpose CPU
- High-speed 16-bit (V850, V850ES CPU), 32-bit (V850E1 CPU) multiply/sum-of-products
  (Multiply: 1 to 2 clocks, sum-of-products: 3 clocks)
- Effective for filter operations and matrix operations for feedback calculations in speed, position, and other servo control.

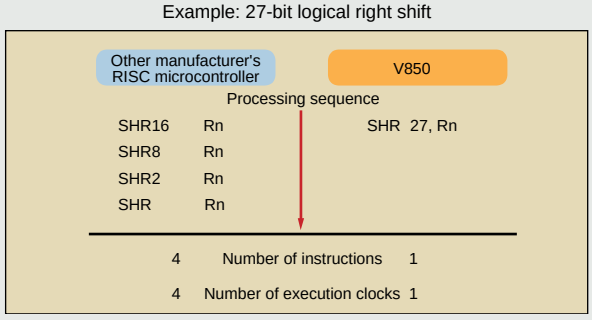


32-bit barrel shifter

V850 Series can realize bit manipulations frequently used during signed data and image data processing in 1 instruction per clock.

- Shifting of any number of bits (0 to 31) executable in 1 instruction per clock
  Improved execution speed/object efficiency
  Effective for extracting arbitrary bit lengths of image data and signed data (extracting code during MH/MR/MMR encoding, etc.)

Example: 27-bit logical right shift



V850E1, V850ES Architecture

The V850E1 and V850ES cores achieve high performance and higher code efficiency through the implementation of the following improvements to the V850 CPU core.

Non-blocking load/store

- Improved bus use efficiency
- Shorter interrupt insensitivity period

Addition of branch/load pipes

- 2-clock branching
- Parallel execution of instructions

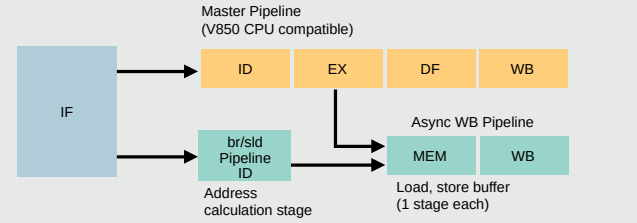
Shift to 3-operand manipulations in 1 slot

- Improved absolute performance
- Example: Synchronous processing of mov + add

Addition of high-level language-compatible instructions

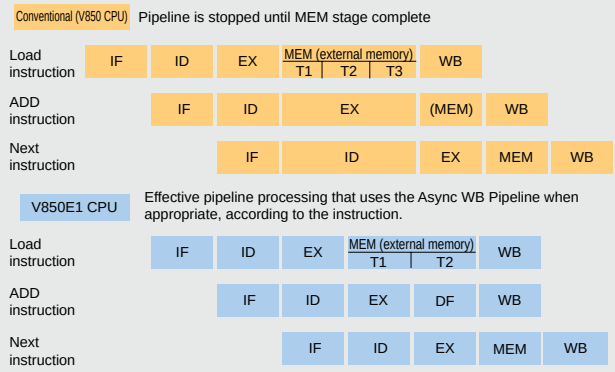
- Improved code efficiency
- 10 to 15% improvement in object efficiency mainly when C compiler used

Pipeline configuration



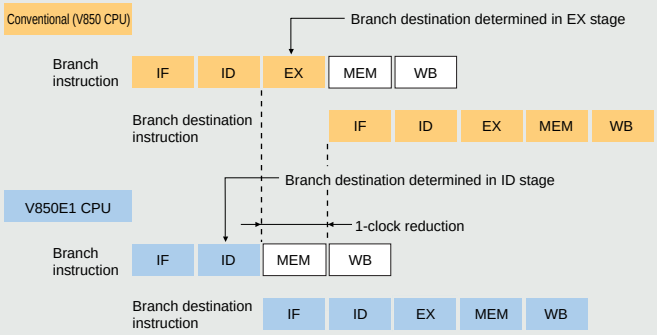
IF (Instruction fetch) : Fetches instructions and increments the fetch pointer.
ID (Instruction decode) : Decodes instructions, creates immediate data, and reads registers.
EX (ALU, multiplier, barrel shifter execution) : Executes decoded instructions.
MEM (Memory access) : Accesses memory of corresponding addresses.
WB (Writeback) : Writes execution results to registers.
DF (data fetch) : Transfers execution data to WB stage.

Non-blocking load/store

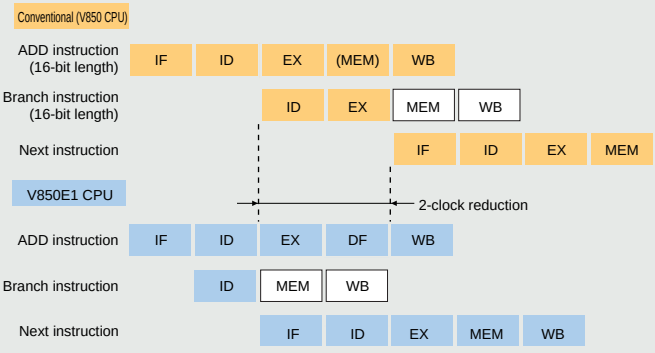


Addition of branch/load pipes

•Pipeline operation with branch instruction

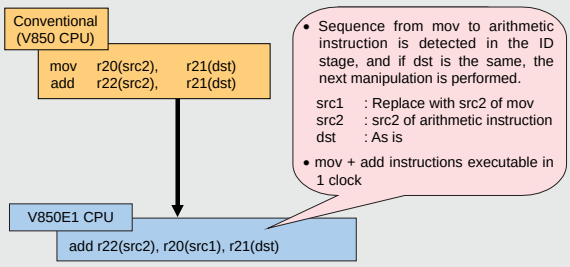


•Parallel instruction execution (when executed by internal ROM)



* The next branch instruction code is also fetched due to the internal 32-bit bus.

Shift to 3-operand manipulations in 1 slot



Addition of high-level language compatible instructions

The V850E1 and V850ES cores have enhanced the instruction set of the V850 core as follows.

◆ switch (2 bytes)
- C language switch statement processing converted into instruction

◆ callt (2 bytes)/ctret (4 bytes)
- Table-reference branching
- Reducing size of call code that frequently appears

◆ Data conversion instructions (2 bytes)
- char, short type cast executed with 1 instruction
- sxh, sxb, zxb, and zxh instructions

◆ prepare/dispose (4 bytes)
- Function start/end processing executed in 1 instruction

◆ unsigned Load
- Reduction of unsigned manipulation code

◆ mov imm32, reg (6 bytes/2 clocks)
- Reduction of address setting code

◆ mul/mulu (4 bytes)
- Reduction of array address calculation
- Improvement of sum-of-products performance

◆ Other
- Bit manipulation (register indirect bit specification)
- cmov (Conditional Move), divide (div/divu/divhu)
- sasf, endian conversion

V850E2 Architecture

V850E2 core features

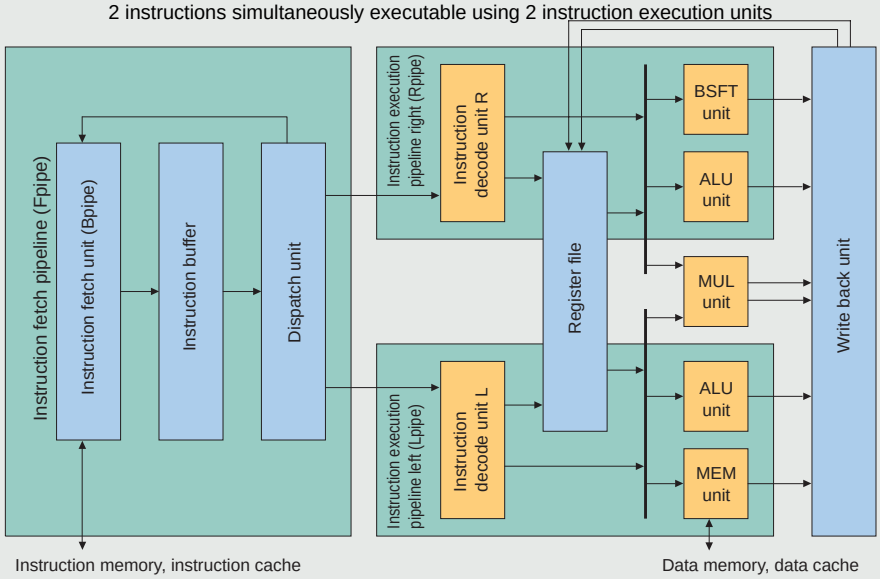
- Real-time performance of 250 MIPS
  - Operation at over 200 MHz
- Inheritance of V850E1 performance and features
  - Upward instruction compatibility with V850E1 and V850ES cores at object level
  - Use of 7-stage pipeline
  - Parallel pipeline configuration (2 parallel superscalar)
  - 128-bit instruction fetch bus
- Support of expanding application software sizes
  - Address space (program/data) expansion
  - Strengthened cache memory support

V850E2 core Main added functions

- 32-bit relative branch instruction
  - Support of program space expansion
  - Long-distance branching performance, elimination of code efficiency losses
- 3-operand instructions (addition of target operations)
  - Higher speed processing of operations such as multiplex add/subtract (64-bit operation, saturate operation) and bit shift, contributing to higher code efficiency
- Sum-of-products instruction
  - Higher speed 32-bit sum-of-products operation (32 × 32 + 64→64 bits)
- Bit search instruction
  - Bit row change point search for run length measurement, contributing to increased speed of conversion from integers to floating decimals, etc.

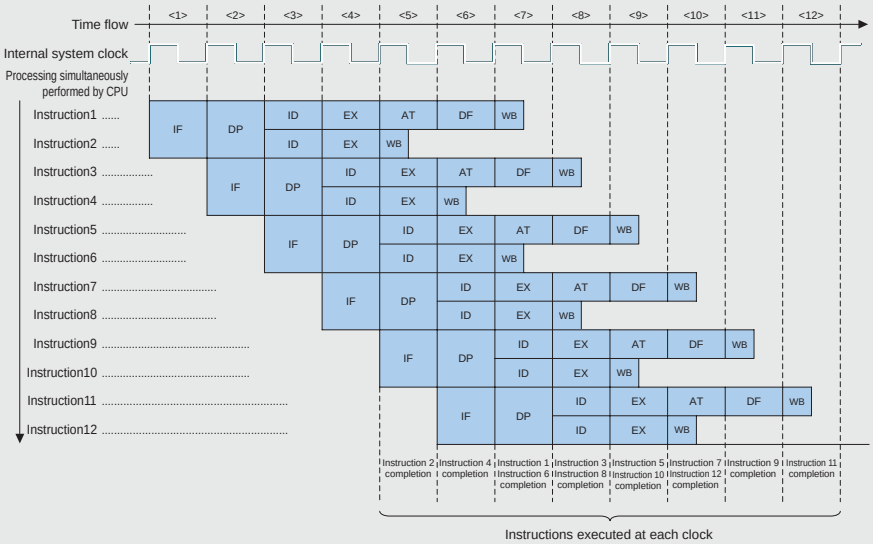
V850E2 core CPU pipeline configuration

2 instructions simultaneously executable using 2 instruction execution units



V850E2 core CPU pipeline operation

Execution of up to 2 instructions/clock possible (dependent on instruction set)



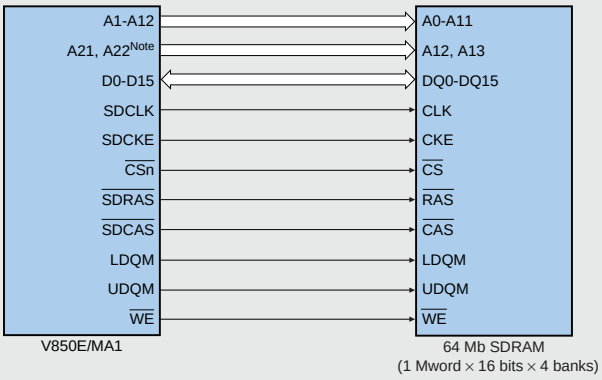
IF : Instruction fetch
DP : Dispatch
ID : Instruction decode
EX : Instruction execution
AT : Address transfer
DF : Data fetch
WB : Writing execution result to register

Memory Access Functions

SDRAM controller

Products: V850E/MA1, MA2, MA3, ME2

- ◆SDRAM connectable without external circuit
- ◆CAS latency: 2, 3 supported
- ◆CBR (automatic) refresh: Self refresh supported

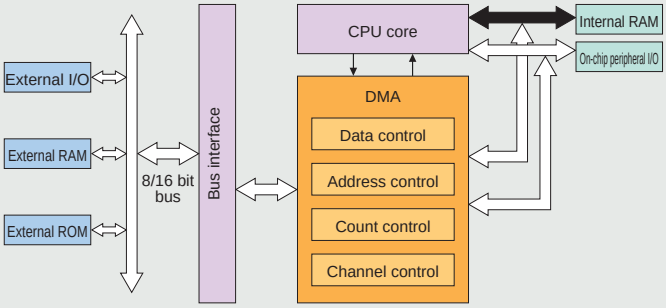


Note The address signal used differs depending on the SDRAM product.

DMA controller (provided in V850E products)

Products: V850E/MA1, MA2, MA3, MS1, MS2, IA1, IA2, IA3, IA4, ME2, SV2

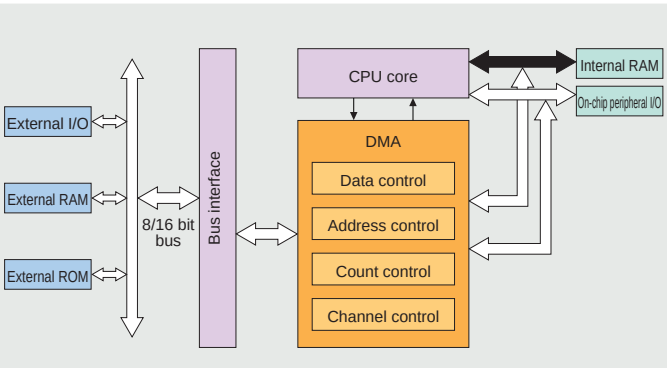
- ◆Transfer targets: Memory-peripheral I/O, memory-memory
- ◆Transfer mode: Single, single step, block transfer
- ◆Transfer units: 8/16 bits
- ◆ Transfer type: 1-cycle transfer, 2-cycle transfer
- ◆Number of transfers: 65536 Max.



DMA controller (provided in V850ES products)

Products: V850ES/SA2, SA3, SG2, SJ2, KG1+, KJ1+, FG2, FJ2
μPD703229Y, 70F3229Y

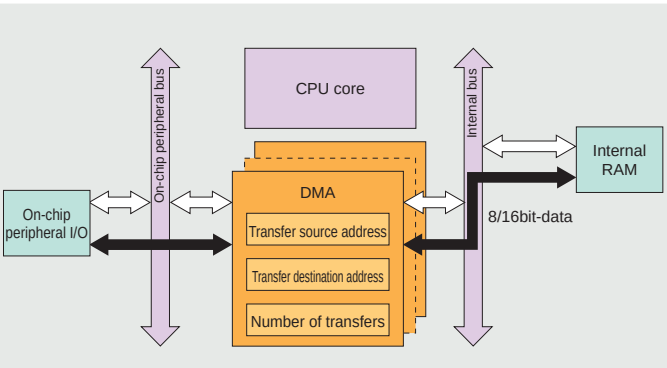
- ◆Transfer targets: Memory-peripheral I/O, memory-memory
- ◆Transfer mode: Single
- ◆Transfer units: 8/16 bits
- ◆Transfer type: 2-cycle transfer
- ◆Number of transfers: 65536 Max.



DMA controller (provided in V850/Sxx products)

Products: V850/SA1, SB1, SB2, SV1, SF1, SC1, SC2, SC3

- ◆Transfer targets: Internal RAM-on-chip peripheral I/O
- ◆Transfer mode: Single
- ◆Transfer units: 8/16 bits
- ◆Transfer clock: 4 clocks Min.
- ◆Number of transfers: 256 Max.

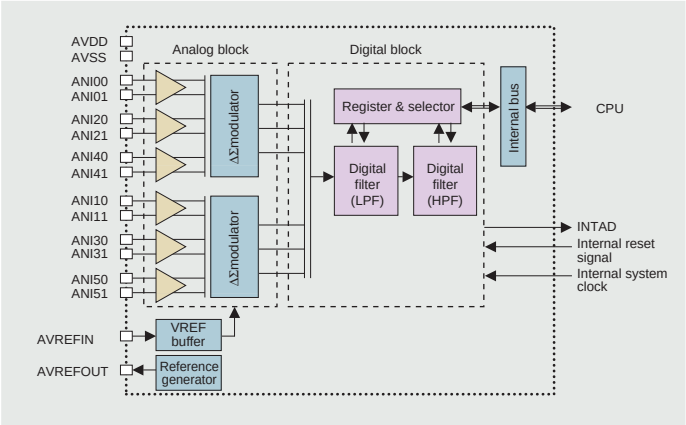


Analog Circuits

ΔΣA/D converter

Products: V850ES/PM1

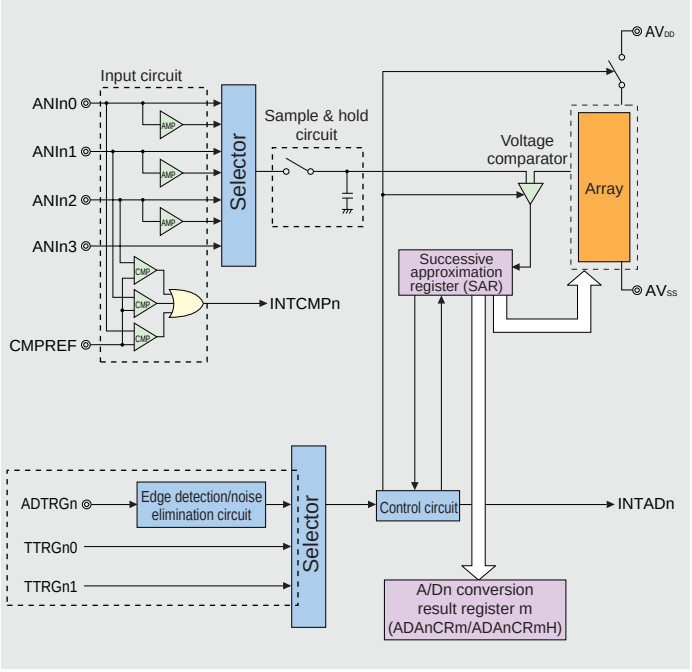
- ◆High-accuracy 16-bit resolution
- ◆Sampling frequency selector (4.340 kHz/2.170 kHz)
- ◆Support of up to 3 lines and 4 phases through multiple input channels



High-speed A/D converter

Products: V850E/IA3, IA4

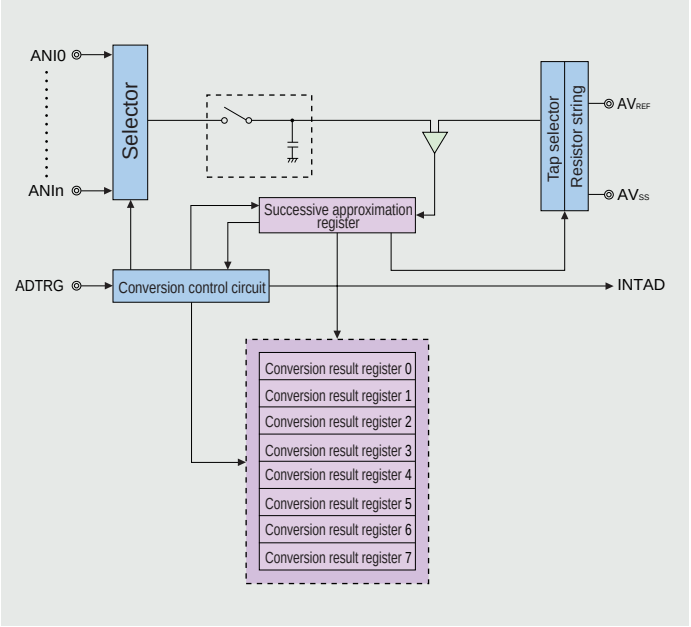
- ◆Simultaneous 10-bit A/D converter sampling for 2 circuits
- ◆On-chip operational amplifier (2.5 ×/5 ×) for input level amplification
- ◆On-chip overvoltage detection comparator



A/D converter (multi-stage buffer type)

Products: V850E/MA1, MA3, ME2, IA1, IA2, MS1, SV2, V850/SV1, V853, etc.

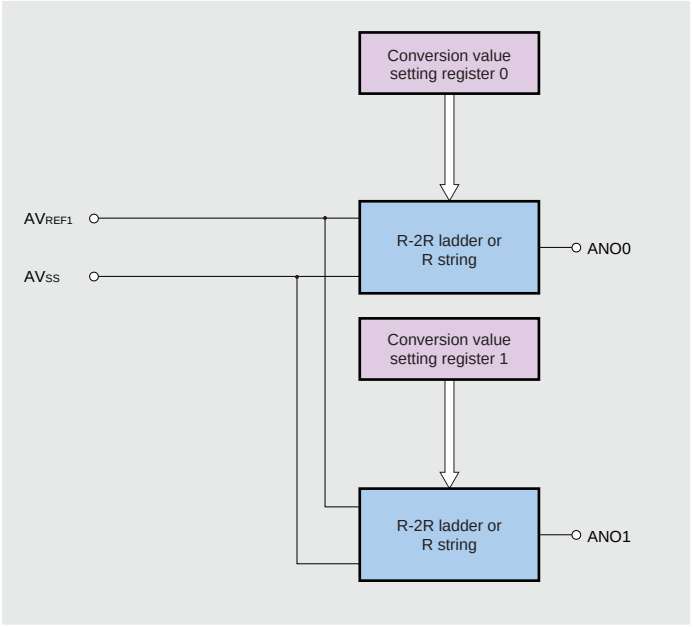
- ◆Conversion startable by software or hardware
- ◆8 on-chip conversion result registers (24 for SV2)
- ◆Select/scan mode switching possible



D/A converter

Products: V850ES/KG1, KJ1, KG1+, KJ1+, SA2, SA3, SG2, SJ2, V850E/MA3, V853

- ◆R-2R ladder method (except for V850ES/SA2, SA3)
- ◆R string method (V850ES/SA2, SA3 only)
- ◆8-bit resolution
- ◆Operation mode: Normal mode/real-time output mode

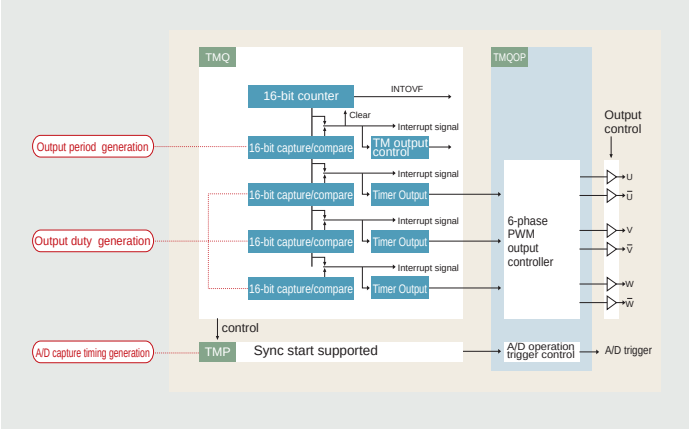


Timer/Counter

Timer configuration during inverter control

Products: V850E/IA3, IA4, MA3, V850ES/IK1

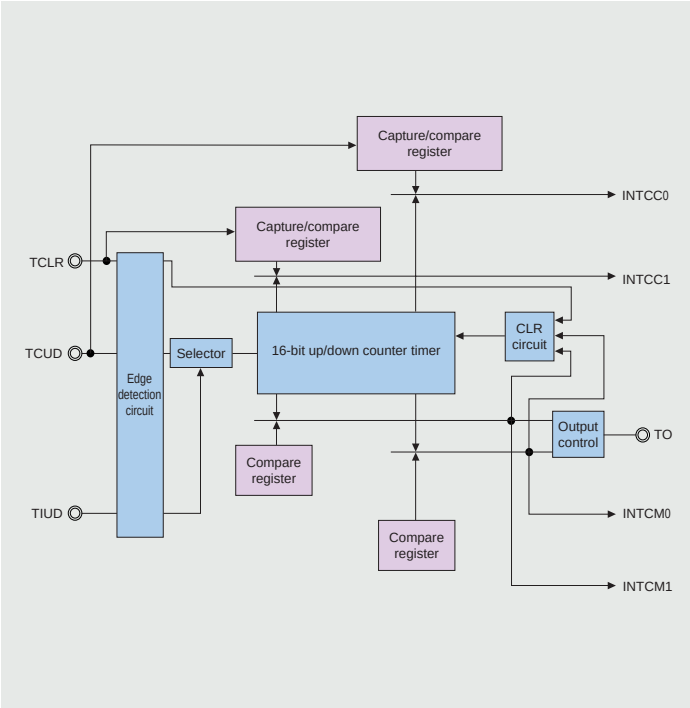
- ◆0% and 100% output and 6-phase PWM output with deadtime possible
- ◆Switchable anytime/batch overwrite for compare register
- ◆A/D converter conversion start trigger generator



Up/down counter

Products: V850E/IA1, IA2, IA3, IA4, MA3, ME2

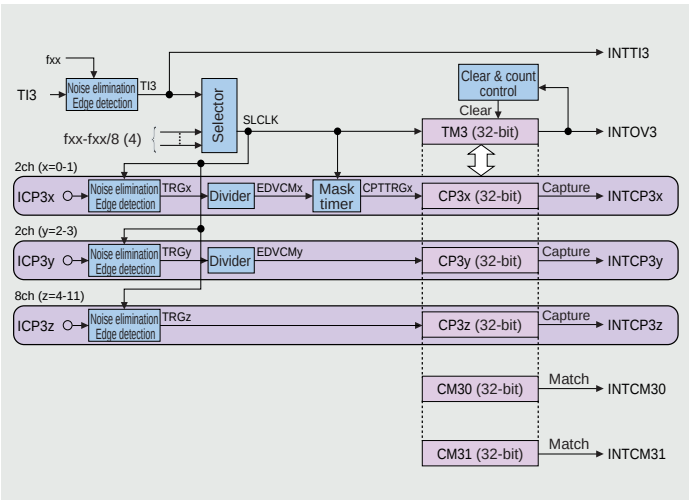
- ◆16-bit 2-phase encoder input possible
- ◆Compare registers: 2
  Capture/compare registers: 2



32-bit servo timer

Products: V850E/SV2

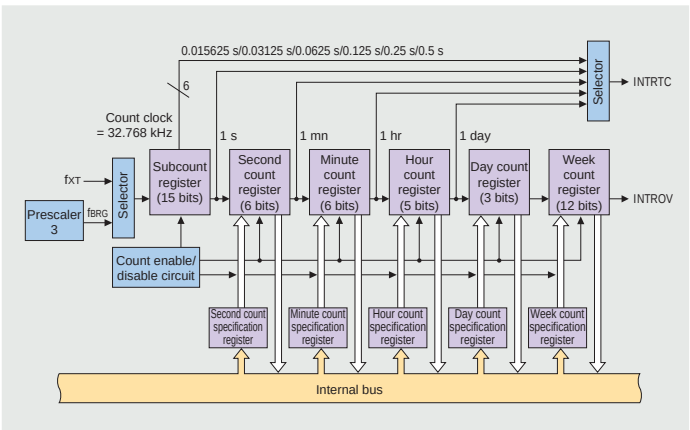
- ◆32-bit timer unit for servo control
- ◆Capture registers: 12
  Compare registers: 2
- ◆External input detection circuit with 1 to 256 dividers
- ◆On-chip 8-bit mask timers: 2



Real-time counter

Products: V850ES/SA2, SA3, PM1

- ◆On-chip week, day, hour, minute, second counters
- ◆Counting up to 4095 periods
- ◆Support of interval interrupt generation at fixed intervals selectable from: 0.015625 s, 0.03125 s, 0.0625 s, 0.125 s, 0.25 s, 0.5 s, 1 s, 1 mn, 1 hr, 1 day

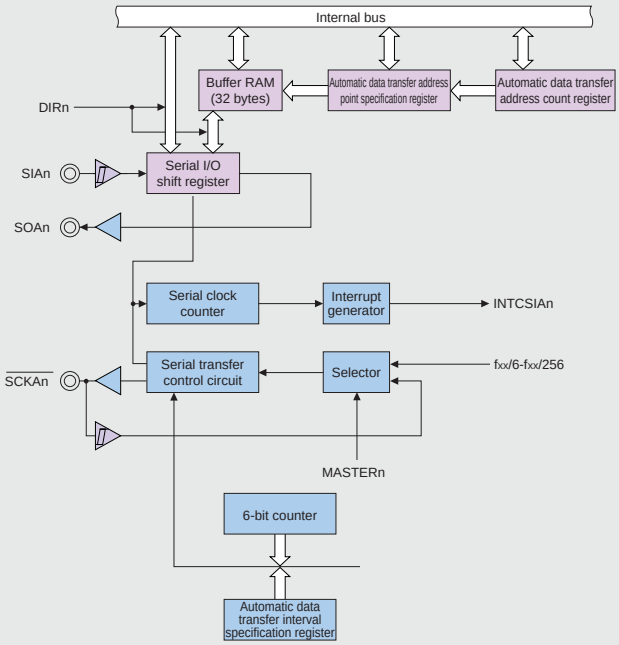


Serial Interface

Serial interface with automatic send/receive function

Products: V850E/SV2, V850ES/KF1, KG1, KJ1, KF1+, KG1+, KJ1+

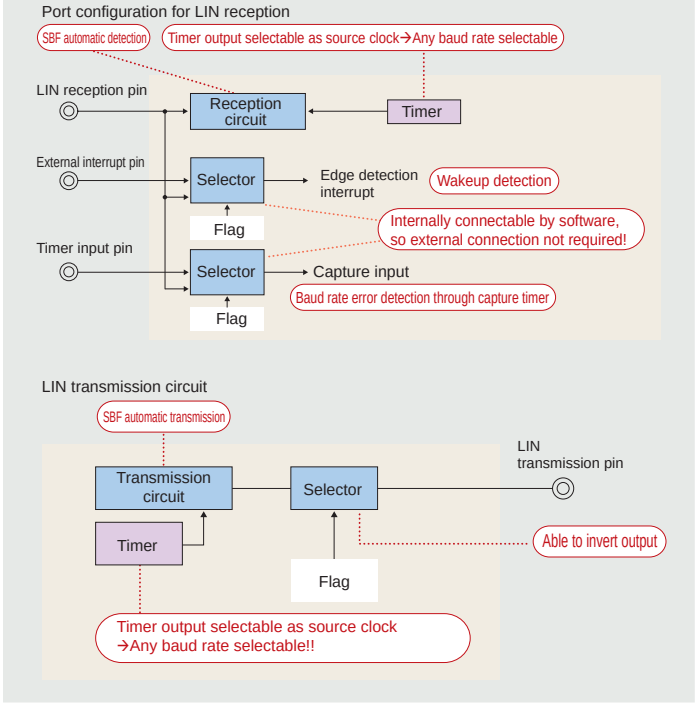
- ◆32-byte internal buffer RAM
- ◆Automatic send/receive function
  - •1 to 32 bytes of transfer bytes specifiable
  - •Transfer interval specifiable (0 to 63 clocks)
  - •Single transfer/repeated transfer specifiable



LINBus

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2

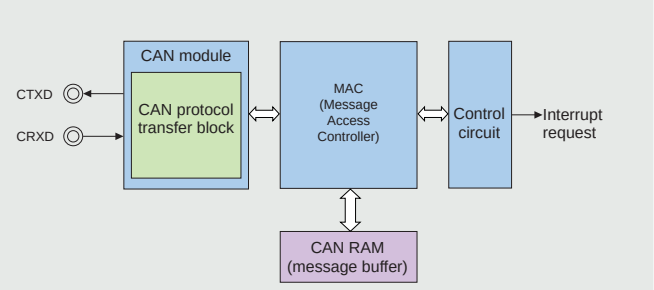
- ◆Low-cost 1-line network bus
- ◆Sync break field (SBF) send/receive possible through hardware
  (Send: 13 bits ≤ SBF ≤ 20 bits; Receive: SBF ≥ 11 bits)
- ◆Also generally usable as UART



CAN

Products: V850ES/SG2, SJ2, FE2, FF2, FG2, FJ2, V850E/IA1, V850/SF1, SC3, DB1

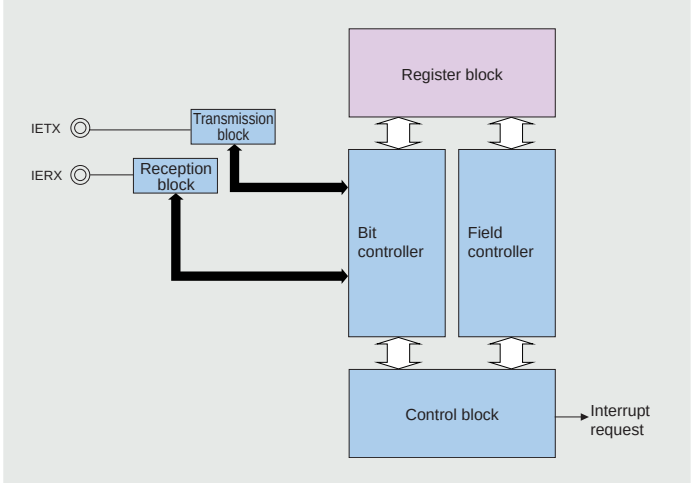
- ◆CAN protocol ver. 2.0 Part B (send/receive of standard and extended frames)
- ◆Max. transfer rate: 500 kbps (V850/DB1 only) 1 Mbps
- ◆32 message buffer



IEBus controller

Products: V850ES/SG2, SJ2, V850/SB2, SC2

- ◆Communication mode 1 supported
- ◆Max. transfer bytes: 32 bytes/frame
- ◆Max. transfer speed: Approx. 17 kbps

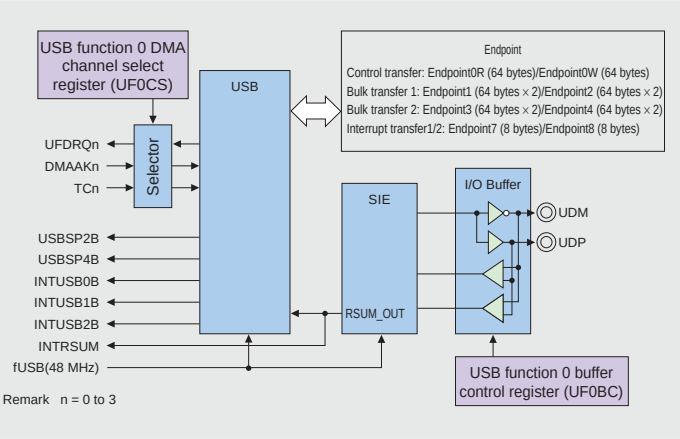


Other

USB

Products: V850E/ME2

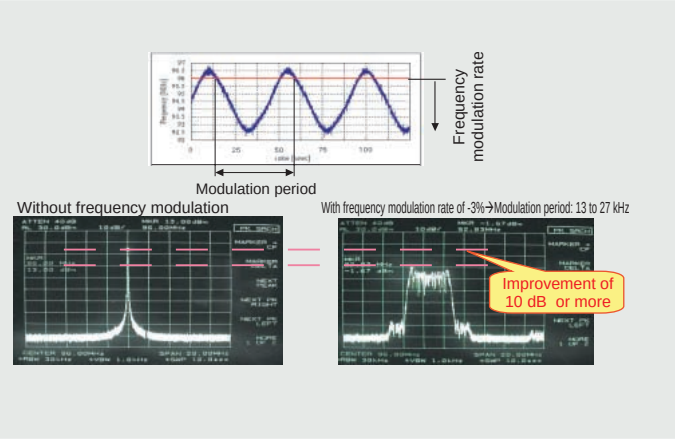
- ◆Compliant with Universal Serial Bus Specification
- ◆Support of 12 Mbps (full speed) transfer
- ◆Many endpoint configurations



SSCG function *(Spread spectrum Frequency Synthesizer Clock Generator)*

Products: V850E/ME2

- ◆EMI peak noise reduction through input frequency modulation
- ◆Large reduction in noise countermeasure time and cost possible
- ◆Frequency modulation rate and modulation period changeable by register setting

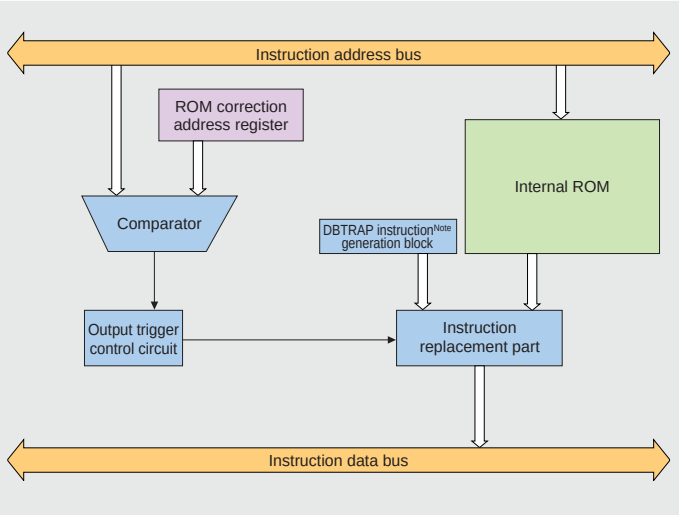


ROM correction function

Products: V850 core :V850/SB1, SB2, SV1, SF1, SC1, SC2, SC3
V850E, V850ES cores :V850ES/SA2, SA3, SG2, SJ2, KE1, KF1, KG1, KJ1, KE1+, KF1+, KG1+, PM1, IK1, μPD703229Y, 70F3229Y, V850E/MA3, SV2, IA3, IA4

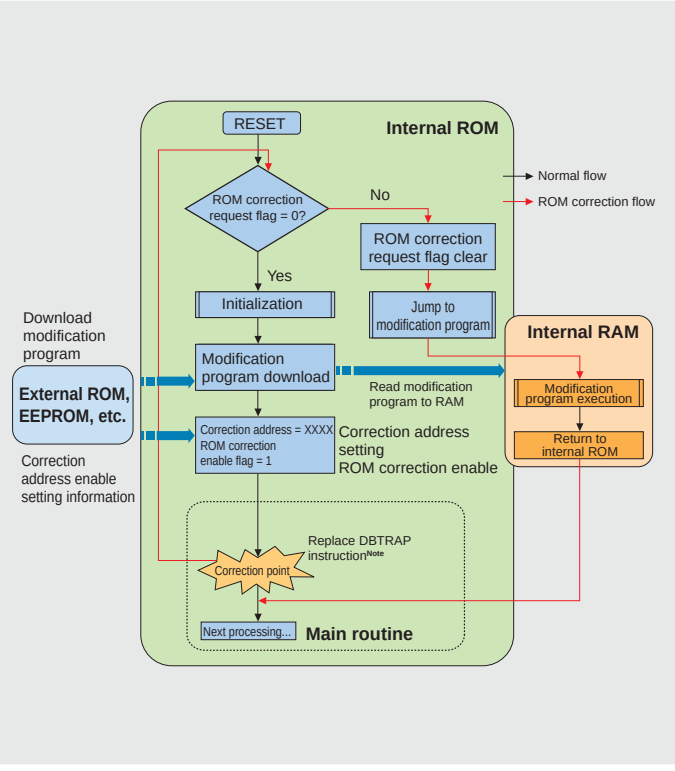
- ◆Instructions of address to be modified inserted to replace DBTRAP instruction (JMP r0 instruction in case of V850 core), branching to 0060H (0000H in case of V850 core)
- ◆Program modification following switch to mask ROM possible
- ◆Modified addresses: 4 points, 8 points[Note]

Note V850E/SV2



Note JMP r0 instruction for the V850 core

Explanation of ROM correction operation

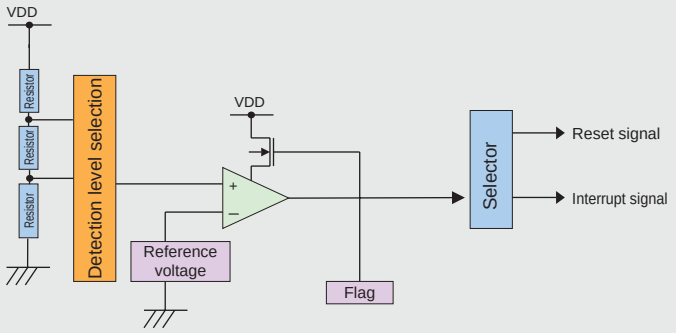


Note JMP r0 instruction in case of V850 core

Low-voltage detection circuit (LVI)

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

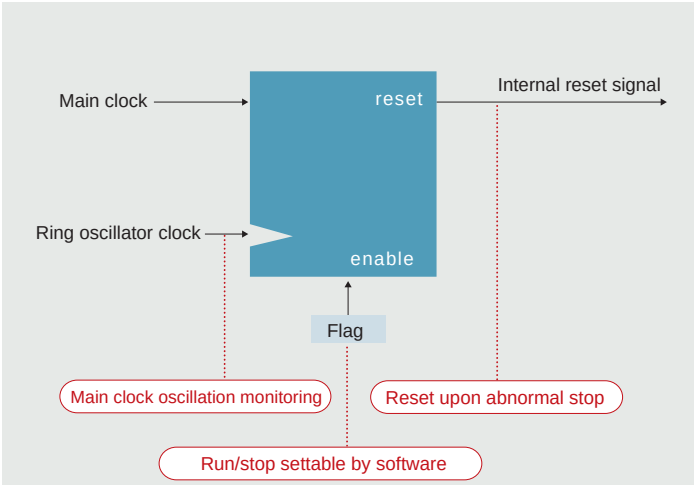
- ◆Detection voltage level changeable by software
- ◆Usable instead of reset IC, contributing to lower system cost
- ◆Detection voltage not changeable after mode transition (security protection)



Clock monitor function

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

- ◆Monitors abnormal stops of main clock with internal Ring- Oscillator
- ◆During abnormal stop, entire system can be set to reset status
- ◆Prevention of destruction due to system deadlock or runaway

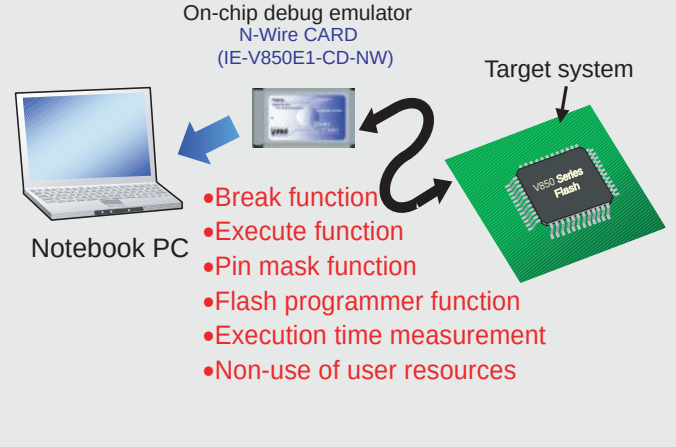


On-chip debugging function

Products: V850E/ME2[Note], V850E/MA3, IA4, SV2, V850ES/KJ1, KJ1+, SG2, SJ2, FE2, FF2, FG2, FJ2, µPD70F3229Y

- ◆Realization of on-chip debugging of microcontroller with DCU (Debug Control Unit)
- ◆Compact and low-cost PC card-type emulator
- ◆Flash programmer function
- ◆Integrated debugger (ID850) supported

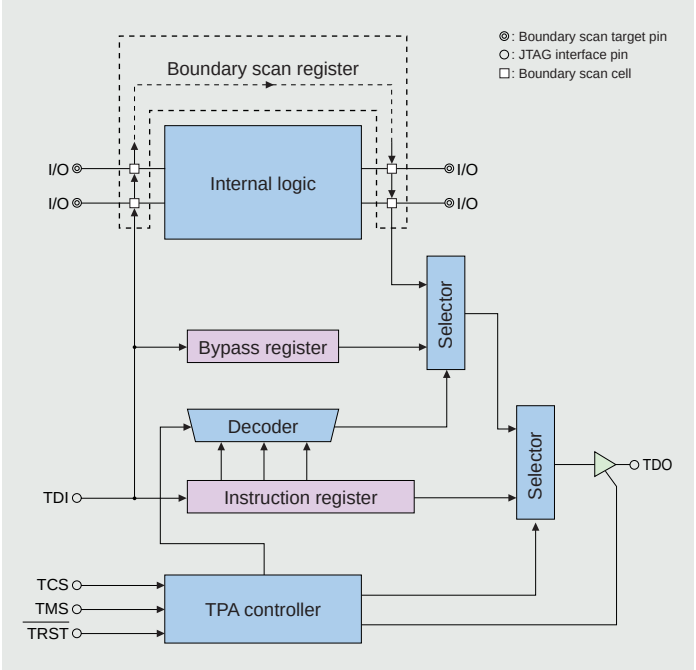
Note Trace function support is possible by using the RTE-2000-TP made by Midas Lab Co., Ltd., or PARTNER-ET II, PARTNER-J made by Kyoto Micro Computer Co., Ltd.



Boundary scan function

Products: V850E/SV2

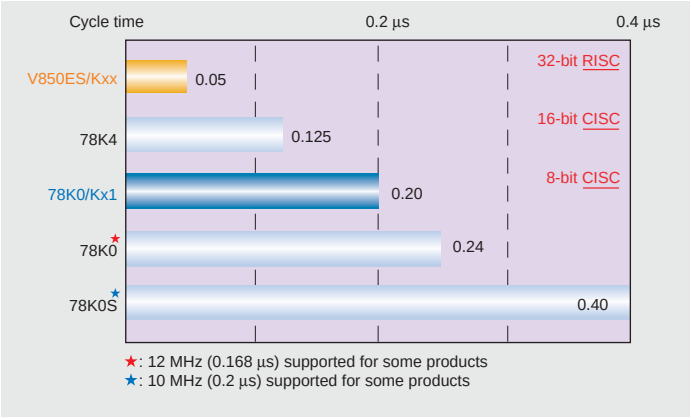
- ◆Use of JTAG (Joint Test Action Group) communication specifications, IEEE1149.1 compliant
- ◆Progressive scan of device's external I/O pins, test data input/output possible
- ◆Connection check of devices soldered on user board possible



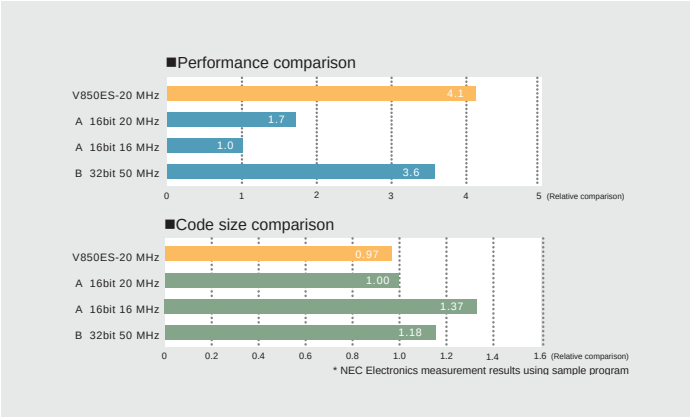
V850 Series Benchmark

The V850 Series realizes high speed, high performance, and high code efficiency.

Minimum instruction execution time



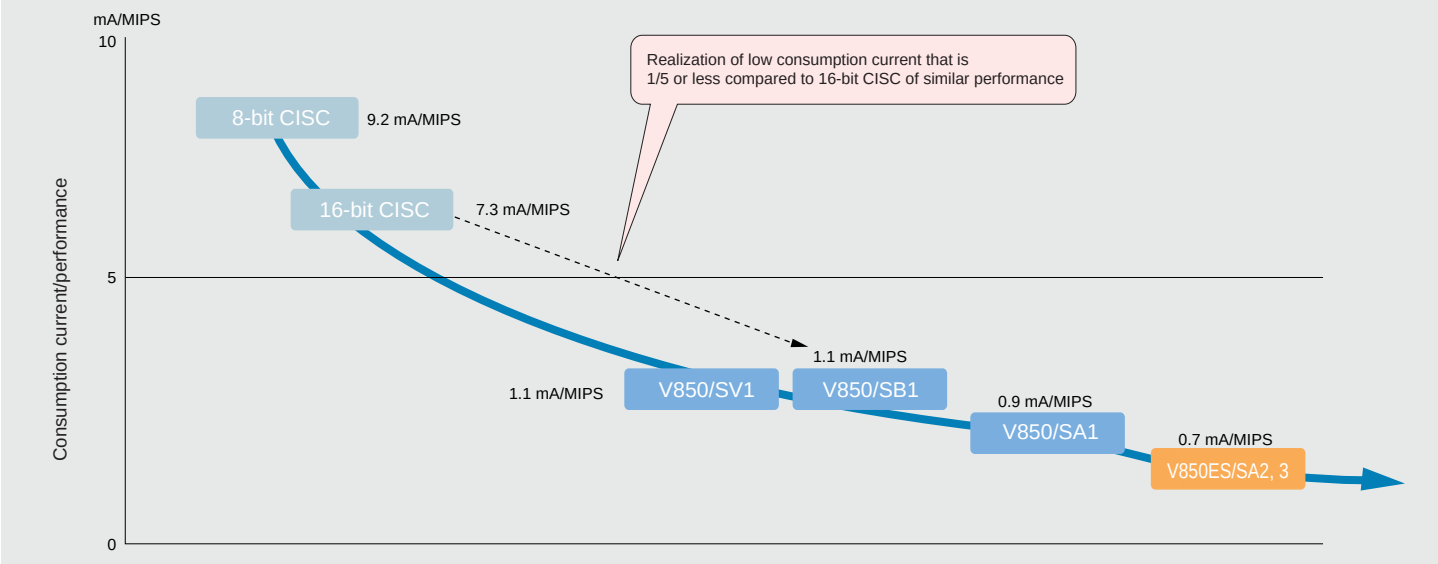
V850 Series performance



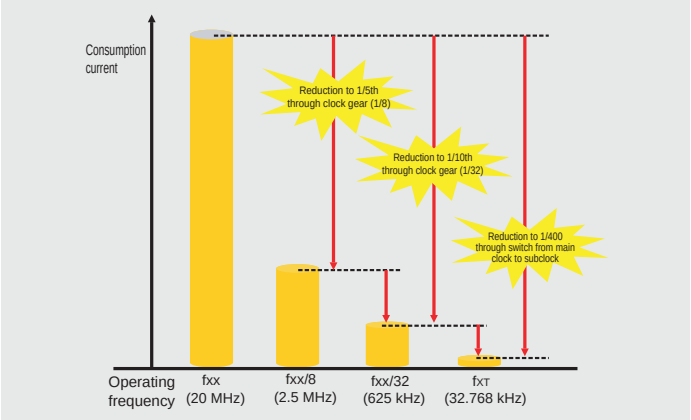
Low Power Consumption

Thanks to thorough energy-saving design, a superior current/performance ratio of 1.1 to 0.7 mA/MIPS is realized, particularly for V850ES and V850/Sxx products. As a result, a reduction in power consumption to 1/5 or less compared to 16-bit CISC microcontrollers of similar performance is realized. Lower system power consumption and higher performance are simultaneously realized through this extremely high power performance.

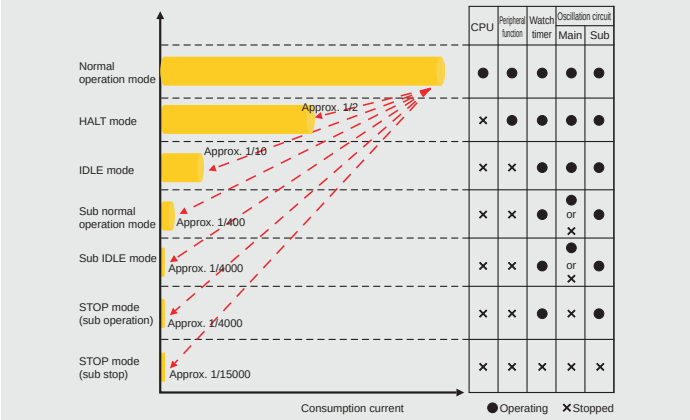
Power performance



Clock gear function



Standby mode

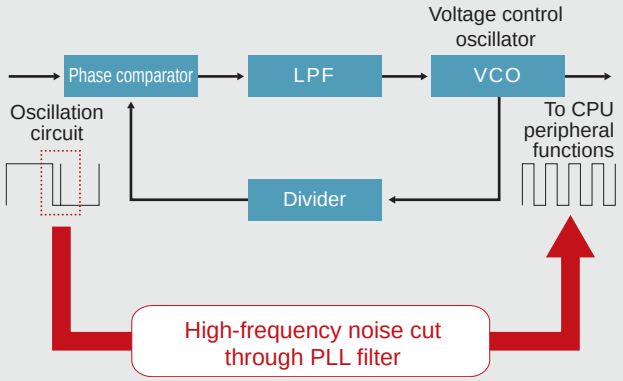


Low Noise Countermeasures

Minimizing the influence of electromagnetic interference (EMI) emitted from the microcontroller and the influence of noise applied to the microcontroller (EMS) is a high priority, particularly for AV equipment such as car audio systems, and thus superior noise performance is required of microcontrollers. Various noise countermeasures are implemented in the V850 Series, and noise performance equivalent or superior to that of 16-bit products has been realized.

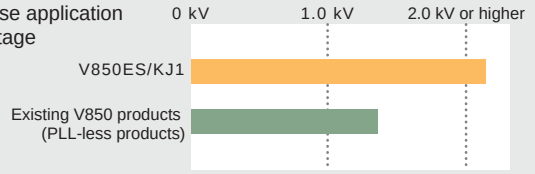
EMS countermeasures

■Use of PLL for oscillation circuit



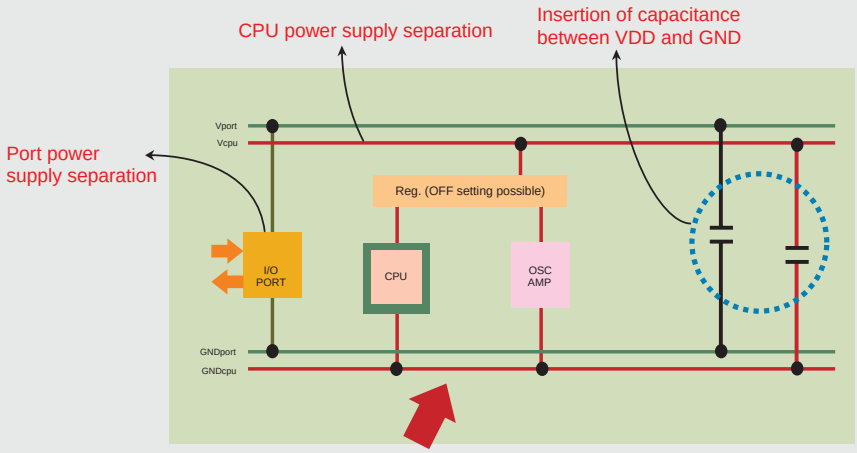
EMS measurement results (power supply coupling measurement)

■Noise application voltage



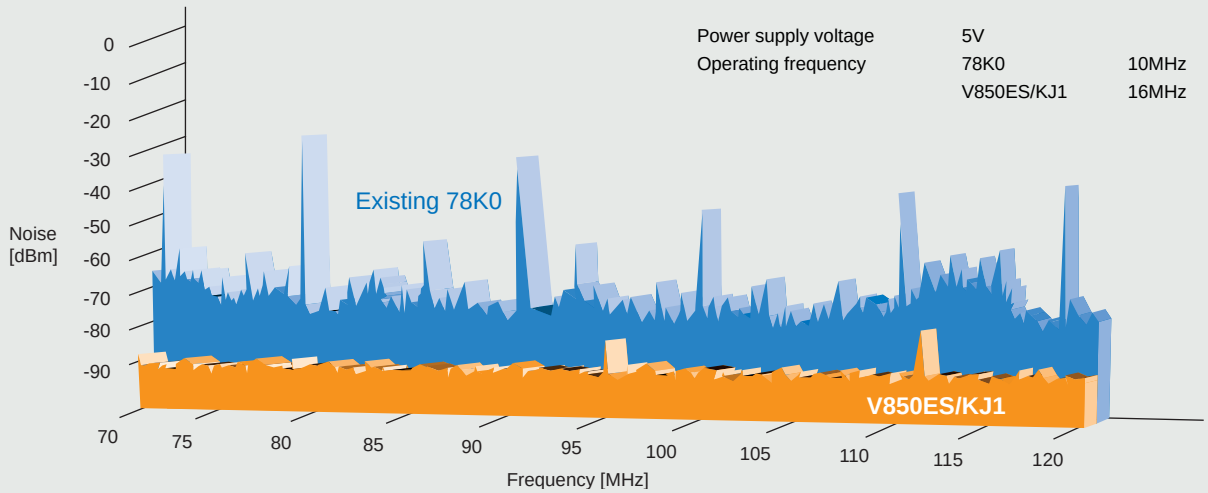
V850ES/KJ1 (flash version)	Existing V850 products
V_{DD}=5 V	V_{DD}=5 V
Resonator: 4 MHz	Resonator: 16 MHz
Internal operation frequency: 16 MHz (PLL = ON)	Internal operation frequency: 16 MHz

EMI noise countermeasures: Power supply circuit countermeasures



Due to the relation between the power supply and GND pad positions and the lead frame, placement is done so as to lower the power supply impedance.

EMS noise measurement results

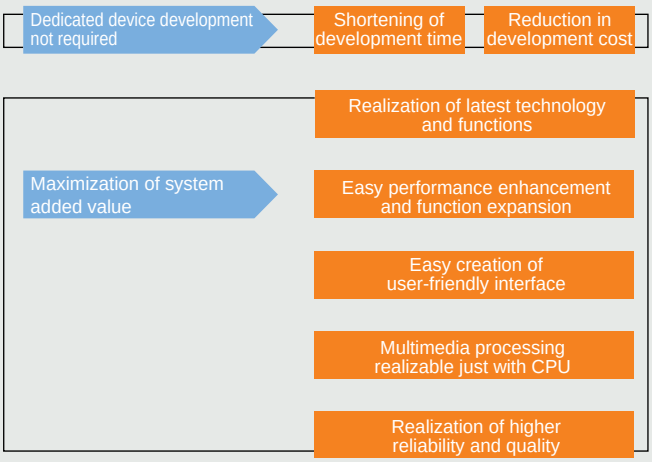


V850 Series Middleware List

Middleware plays a major role for maximizing processor performance and realizing high-speed processing of complex data with flexibility and ease.

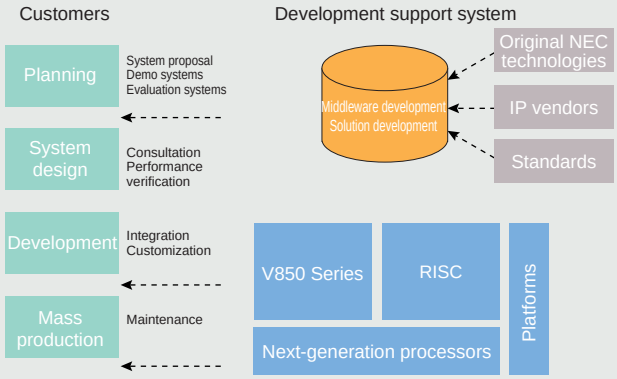
NEC Electronics offers a large array of middleware that is optimized for the CPU architecture and importantly contributes to shortening development time, while also facilitating additions and changes to dedicated functions whose implementation as hardware for devices, etc., used to have high cost and time requirements, and the creation of user-friendly interfaces.

Middleware merits:



Shift to middleware accelerating deployment to optimum processors

An increasing number of processors optimized for various systems and based on NEC Electronics' original technology and the superb technology of third parties, as well as other technologies that have been established as standards, are being deployed from.



Middleware product list

Category	Middleware		V850 Series
Image	JPEG		◎
	MPEG-4/H.263 Video		—
Speech	Text To Speech	Japanese	◎
	Speech CODEC	G.723.1 Annex A/C	—
		G.726 (ADPCM)	◎
		G.729 Annex A/B	—
		AMR	—
		MPEG-4 CELP	—
	Acoustic echo canceller (for hands-free operation)	AEC	—
	Noise suppressor	3GPP-NS	—
Sound	Audio decoder	AAC	—
		MP3	—
		WMA	—
	Sound generator for cellular phone ringer melody		—

Category	Middleware		V850 Series
Recognition	Speech recognition	Japanese (large vocabulary)	—
		Japanese (small vocabulary)	◎
		Chinese (small vocabulary)	◎
		English (small vocabulary)	◎
	Handwriting recognition	Japanese (input frame required)	◎
		Japanese (input frame not required)	—
Security	Encryption	CIPERUNICORN	◎
	Fingerprint recognition		◎
Internet	TCP/IP		◎
Storage	PC-compatible file system		◎

◎ : Development completed

Middleware performance list

Middleware	Performance	Power (MIPS)	ROM	RAM
JPEG	QVGA×24 : Enc0.32s/Dec0.24s	–	17.5 KB	15 KB
G.726 (ADPCM)	32Kbps, 16Kbps	Enc8/Dec8.2	9 KB	80 B
Speech recognition (small vocabulary)	0.4s	19 (20 words)	82 KB	3.5 KB (15 words)
		63 (100 words)		

Speech Recognition

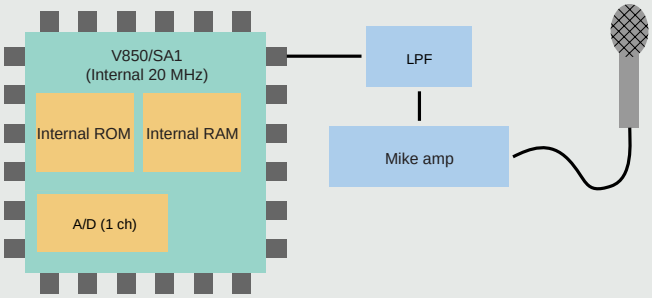
Speech recognition is realized on a single chip using the memory and peripheral I/Os in the V850 Series. Ideal for applications such as games and home appliances that must feature speech recognition but are subject to large restrictions.

- Realization of speech recognition with memory and peripheral I/Os contained in V850 Series
- Expansion of number of recognized words

  Recognized number of words: 30 words (in case of V850/SA1, 20 MHz)

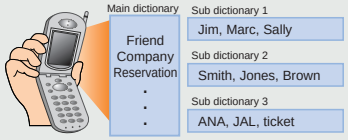
V850 Series

Speech recognition system configuration example



- Realization of speech recognition using only memory and peripheral I/Os contained in V850 Series
- Expansion of number of recognized words

Expansion of number of recognized words



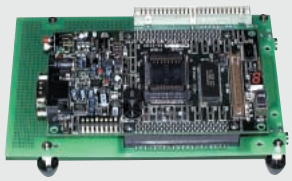
Memory capacity

ROM/RAM	Description	Capacity
ROM	Program	26 KB
	Data	40 KB
ROM/RAM mix	Recognition dictionary (in case of 15 words)	0.5 KB
RAM	Work area (in case of 15 words)	3.4 KB
	Stack	0.3 KB

Recognition dictionary and work vary depending on the number of recognized words.

- Speech recognition evaluation system

  NEC Electronics provides an environment allowing easy evaluation for the introduction of speech recognition.
  For details and the purchasing method, consult your NEC Electronics sales representative.



JPEG

- Conforms to JPEG international standard

  Conforms to DCT baseline process (non-reverse coding)
- Versatile compression and decompression processing

  <Compression functions>
  - •User-customizable VRAM input module
  - •User-specified Huffman and quantization tables
  - •APPn marker insertion
  - •Compression suspend function

  <Decompression processing>
  - •User-customizable VRAM output module
  - •Support of various JPEG markers (DRI, RSTn, DNL)
  - •Decompression suspend function

JPEG performance

CPU	Sample Ratio	Processing Time			
		QVGA (320×240×24)		VGA (640×480×24)	
		Compression	Decompression	Compression	Decompression
V850E/MS1 (33MHz)Note	4:1:1 (Quality75)	0.32 s	0.24 s	1.3 s	0.97 s

Note Programs are placed in internal ROM, and stack and (some) work areas are placed in internal RAM. The data and other works are placed in external RAM.

Memory

ROM		RAM	
Compression	Decompression	Compression	Decompression
10 KB	7.5 KB	5 KB	10 KB

Text to Speech (for Japanese Text)

- Speech synthesized from Japanese Kana and Kanji text (SJIS code)
- Versatile speech synthesis

  Synthesis of female voices possible

  Various adjustable parameters such as intonation and reading speed
- Rhythm of synthesized speech (pitch, phoneme duration) can be designed (Speech Designer compatible)

  Speech synthesis using natural rhythm possible (synthesis of more natural sounding speech)
- Support of special characters (Reading of special characters settable in user dictionaries)
- Synthesis speed

  Works also with V850/SA1 (20 MHz). (However, text is placed in internal ROM.)

ROM/RAM	Description	Capacity
ROM	Program	126 KB
	Data	35 KB
	Dictionary data (approx. 80,000 words)	1.2 MB
	Phoneme data	567 KB (8 kHz sampling)
		684 KB (11 kHz sampling)
RAM	Work	160 KB
	Stack	508 bytes
	Speech output buffer	12 KB

Features

To answer the need for shorter development time and maintenance after shipping, NEC Electronics offers microcontrollers with on-chip flash memory available in a large range of capacities from 64 KB to 640 KB as part of the V850 Series. NEC Electronics' flash memory microcontrollers offer the following features.

◆Flash capacity
64 to 640 KB
◆Overwrite unit
Entire memory at one time, or block units
◆Rewrite method
Serial communication with dedicated flash memory programmer (on-board, off-board)
Self-flash programming
◆Rewrite voltage
Single-power-supply flash: Operation voltage
Dual-power-supply flash: Operation voltage
7.8 V/10.3 V
◆Rewrite count:
100 times

Flash microcontroller lineup

Flash Memory Size (bytes)	64K	128K			192K		256K				384K			512K			640K
RAM size (bytes)	4K	4K	6K	8K	12K	16K	8K	10K	12K	16K	16K	24K	32K	20K	24K	32K	48K
V850ES/KE1		◎															
V850ES/KF1		○	◎/○						◎								
V850ES/KG1		○	◎/○							◎							
V850ES/KJ1		○	◎/○							◎							
V850ES/KE1+*		◎															
V850ES/KF1+*			◎						◎								
V850ES/KG1+*			◎							◎							
V850ES/KJ1+*			◎							◎							
V850ES/SG2													◎				◎
V850ES/SJ2													◎				◎
μPD70F3229Y													◎				
V850ES/SA2,SA3										◎							
V850/SA1		○					○										
V850/SB1										○		○			○		
V850/SB2										○		○			○		
V850/SC1,SC2,SC3															○		
V850E/MA3																◎	
V850E/MA1								○									
V850E/MS1		○															
V853		○					○										
V850E/IA3, IA4									◎								
V850E/IA2			○														
V850E/IA1								○									
V850ES/IK1*			◎														
V850ES/FE2*	◎		◎														
V850ES/FF2*			◎						◎								
V850ES/FG2*			◎						◎		◎						
V850ES/FJ2*									◎		◎			◎			
V850E/SV2															◎		
V850/SV1										○	○						
V850/SF1										○							
V850/DB1			○														

◎: Single power supply
○: Dual power supply
◎/○: Single power supply/dual power supply
*: Under development

Rewrite Modes

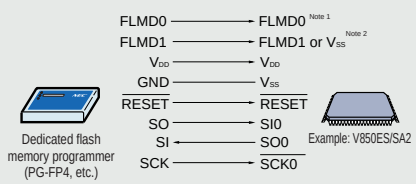
To enable integrated use ranging from development to mass production and maintenance, the V850 Series supports a programmer rewrite mode that uses serial communication supporting on-board programming, as well as a self-programming mode that rewrites flash memory with user programs.

◆On-board programming mode
This programming mode is used to rewrite the flash memory mounted on the target system using a dedicated flash memory programmer.
◆Off-board programming mode
This programming mode is used to rewrite flash memory using a dedicated flash memory programmer and dedicated program adapter (FA Series[Note 1]).
◆Self-programming mode
This programming mode is used to rewrite flash memory by executing the user program written beforehand to the flash memory using on-board/off-board programming.[Note 2]

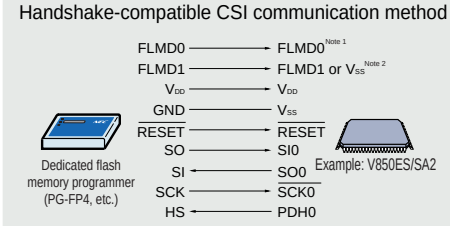
Notes 1. The FA Series is a product of Naito Densei Machida Mfg. Co., Ltd.
2. Since instruction fetch and data access cannot be performed from the internal flash memory area during self-programming, a program for rewriting internal RAM or external memory must be transferred in advance.

Programmer program (on-board/off-board)

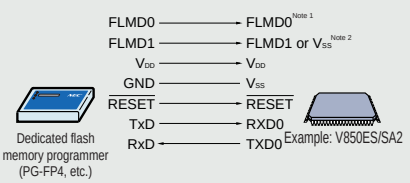
CSI communication method



Handshake-compatible CSI communication method



UART communication method

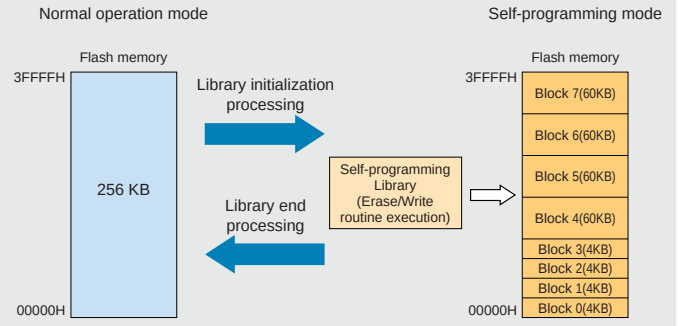


Note 1. In the case of dual-power-supply flash, V_{PP}

Note 2. In the case of dual-power-supply flash, don't connect.

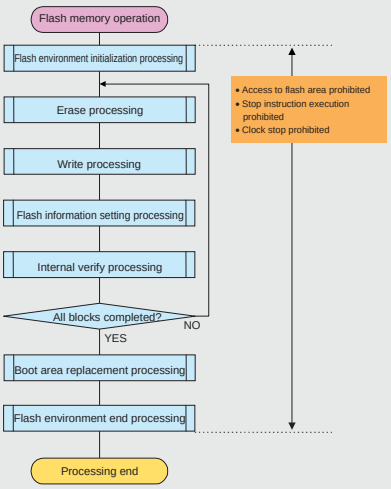
Self-programming mode (single-power-supply method)

Flash memory can be erased and rewritten using a self-programming library from a program placed in an area outside the flash memory.



Caution The number of blocks and block capacity differ depending on the products.
(Example: V850ES/SA2)

Self-programming flow



Flash Specifications List

Category	Part No.	Flash Memory Capacity	Max. Operating Frequency	Rewrite Voltage		Rewrite Mode				Rewrite Count (Times)
						On-Board/Off-Board Programming			Self-Programming	
				V_{DD}	V_{PP}	CSI	UART	CSI+HS		
Low end	V850ES/KE1	128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KF1	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KF1	128 KB	20 MHz	4.5 V to 5.5 V	10.3 V	√	√	√	—	100
	V850ES/KG1	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KG1	128 KB	20 MHz	4.5 V to 5.5 V	10.3 V	√	√	√	—	100
	V850ES/KJ1	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KJ1	128 KB	20 MHz	4.5 V to 5.5 V	10.3 V	√	√	√	—	100
	V850ES/KE1+*	128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KF1+*	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KG1+*	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/KJ1+*	256 KB/128 KB	20 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
Middle range	V850ES/SG2	640 KB/384 KB	20 MHz	2.85 V to 3.6 V	—	√	√	√	√	100
	V850ES/SJ2	640 KB/384 KB	20 MHz	2.85 V to 3.6 V	—	√	√	√	√	100
	μPD70F3229Y	384 KB	20 MHz	3.5 V to 5.5 V	—	√	√	√	√	100
	V850ES/SA2	256 KB	20 MHz	2.2 V to 2.7 V	—	√	√	√	√	100
	V850ES/SA3	256 KB	20 MHz	2.2 V to 2.7 V	—	√	√	√	√	100
	V850/SA1	256 KB/128 KB	20 MHz	3.0 V to 3.6 V	7.8 V	√	√	√	√	100
	V850/SB1	512 KB/384 KB/256 KB	20 MHz	4.0 V to 5.5 V	7.8 V	√	√	√	√	100
	V850/SC1	512 KB	20 MHz	3.5 V to 5.5 V	7.8 V	√	√	√	√	100
High end	V850E/MA3	512 KB	80 MHz	2.3 V to 2.7 V (internal) 3.0 V to 3.6 V (external)	—	√	√	√	√	100
	V850E/MA1	256 KB	50 MHz	3.0 V to 3.6 V	7.8 V	√	√	√	√	100
	V850E/MS1	128 KB	33 MHz	3.0 V to 3.6 V	7.8 V	√	√	—	√	100
	V850E/MS1	128 KB	33 MHz	3.0 V to 3.6 V (internal) 4.5 V to 5.5 V (external)	7.8 V	√	√	√	√	100
	V853	256 KB/128 KB	33 MHz	4.5 V to 5.5 V	10.3 V	√	√	√	—	20
ASSP	V850E/IA4	256 KB	64 MHz	2.3 V to 2.7 V (internal) 4.5 V to 5.5 V (external)	—	√	√	√	√	100
	V850E/IA3	256 KB	64 MHz	2.3 V to 2.7 V (internal) 4.5 V to 5.5 V (external)	—	√	√	√	√	100
	V850E/IA2	128 KB	40 MHz	4.5 V to 5.5 V	7.8 V	√	√	√	√	100
	V850E/IA1	256 KB	50 MHz	3.0 V to 3.6 V (internal) 4.5 V to 5.5 V (external)	7.8 V	√	√	√	√	100
	V850ES/IK1*	128 KB	32 MHz	4.5 V to 5.5 V	—	√	√	√	√	100
	V850E/SV2	512 KB	40.5 MHz	2.3 V to 2.7 V (internal) 2.7 V to 3.6 V (external)	—	√	√	√	√	100
	V850ES/FE2*	128 KB/64 KB	20 MHz	4.0 V to 5.5 V	—	√	√	√	√	100
	V850ES/FF2*	256 KB/128 KB	20 MHz	4.0 V to 5.5 V	—	√	√	√	√	100
	V850ES/FG2*	384 KB/256 KB/128 KB	20 MHz	4.0 V to 5.5 V	—	√	√	√	√	100
	V850ES/FJ2*	512 KB/384 KB/256 KB	20 MHz	4.0 V to 5.5 V	—	√	√	√	√	100
	V850/SV1	384 KB/256 KB	20 MHz	3.1 V to 3.6 V	7.8 V	√	√	√	√	100
	V850/SB2	512 KB/384 KB/256 KB	19 MHz	4.0 V to 5.5 V	7.8 V	√	√	√	√	100
	V850/SC2	512 KB	20 MHz	3.5 V to 5.5 V	7.8 V	√	√	√	√	100
	V850/SC3	512 KB	20 MHz	3.5 V to 5.5 V	7.8 V	√	√	√	√	100
	V850/SF1	256 KB	16 MHz	3.5 V to 5.5 V	7.8 V	√	√	√	√	100
	V850/DB1	128 KB	16 MHz	4.0 V to 5.5 V	7.8 V	√	√	√	√	100

*: Under development

Flash Memory Programmers

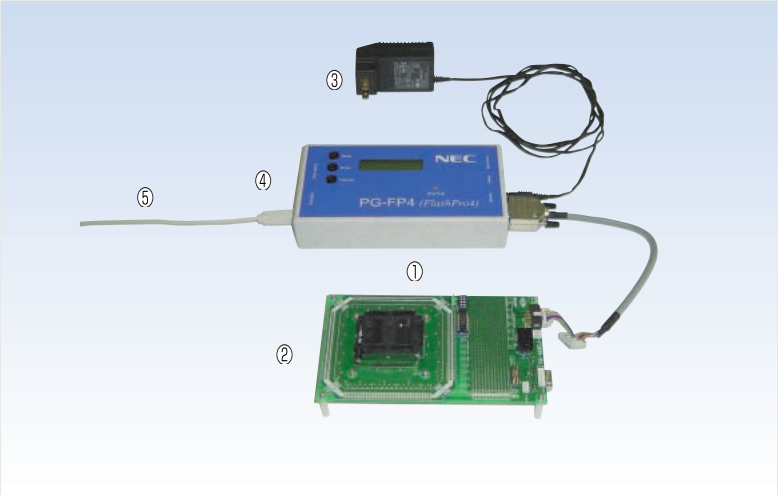
NEC Electronics flash memory programmer: PG-FP4

[Features]
◆Supports write to all NEC Electronics microcontrollers with internal flash memory.
◆USB support through host machine interface
◆Allows verification of various types of information, including programmer setting information, error messages, and check-sum, even in stand-alone configuration, from the main unit's LCD.
◆Enables downloading of two types of user code and selecting of valid code
◆Device-specific information required for writing automatically settable with parameter files
◆Supports both on-board programming and program adapter programming.
◆ Easy-to-carry A5 size
◆Simple operation either on stand-alone basis and on Windows™ 95/Windows 98/Windows Me/ Windows 2000/Windows XP, Windows NT™ 4.0 using a dedicated application (Flashpro4)

●Flash memory programmer configuration

PG-FP4 allows single-microcontroller programming when used with a program adapter (FA Series of Naito Densei Machida Mfg. Co., Ltd.). On-board programming can also be performed.
A sample rewrite environment when using the program adapter is shown below.

Rewrite environment example



① Flash memory program (PG-FP4)
② Target system
③ Power-supply unit
④ Host machine interface (USB)
⑤ To host machine

Cautions 1. Install the PG-FP4 control software and target device parameter file in the host machine.
•PG-FP4 control software: Bundled with PG-FP4
•PG-FP4 parameter file: Distributed via online delivery service
2. In addition to programming using the program adapter, on-board programming on the target system is also possible.

Third-party flash memory programmers (1/2)

●Programming system Y1000-8

[Manufacturer/Distributor] Wave Technology Co., Ltd.

[Target Devices] V850/SV1, SB1 (μPD70F3032B, 70F3033B), SB2 (70F3035B, 70F3037H), V850E/IA1 (70F3116), MA1

[Features]
◆Gang programmer enabling simultaneous programming and verification of up to 8 devices
◆ Enables reading of master data directly from floppy disk to internal memory
◆Data dump display and editing functions
◆Master data storable on internal hard disk
◆Designed for simple and comfortable operation via touch panel, and superior operability via PASS/FAIL display, check-sum display, and task count display supporting sockets.

[Additional information]
TEL : +81-3-5304-1885 FAX : +81-3-5304-1886
E-mail : sales@y1000.com
Website: http://www.y1000.com/index_e.html

Third-party flash memory programmers (2/2)

FlashPRO IV: FL-PR4

[Manufacturer/Distributor] Naito Densei Machida Mfg. Co.

[Target Devices] V850 Series

[Features]

◆Supports writing to all NEC Electronics microcontrollers with internal flash memory.
◆USB support through host machine interface
◆Allows verification of various types of information, including programmer setting information, error messages, and check-sum, even in stand-alone configuration, from the main unit's LCD.
◆Enables downloading of two types of user code and selecting of valid code
◆Device-specific information required for writing automatically settable with parameter files
◆Supports both on-board programming and program adapter programming.
◆Easy-to-carry A5 size
◆Simple operation either on stand-alone basis and on Windows 95/Windows 98/Windows Me/ Windows 2000/Windows XP, Windows NT 4.0 using a dedicated application (Flashpro4)

[Additional information]

TEL : +81-45-475-4191 FAX : +81-45-475-4091
E-mail : info@ndk-m.co.jp
Website: http://www.ndk-m.co.jp/asmis/eng/index.html

NET IMPRESS

[Manufacturer/Distributor] Yokogawa Digital Computer Corporation

[Target Devices] V850/SB1 (μPD70F3033B), SB2(70F3037H), SA1(70F3017A), SC3(70F3089Y), V853(70F3003A, 70F3025A), V850E/MS1(70F3102A), MA1(70F3107), IA1, IA2(70F3114), V850ES/KF1(70F3210), FE2, FF2, FG2, FJ2, SG2, SJ2

[Features]

◆Enables programming of flash memory microcontrollers of various writing specifications solder mounted on user system boards.
◆One control module is the key to this product's versatility.
Microcontrollers of the same family are supported by changing parameters, and microcontrollers of different families are supported by purchasing the required license for the descriptor part.
◆Can be used on standalone basis as well as via a host machine.
◆Rich lineup of downloadable freeware

[Additional Information]

TEL : Japan +81-42-333-6224
U.S.A +408-941-0132 (Yokogawa Corporation of America)
Europe +44-1256-811998 (Ashling Microsystems Limited)
Korea +82-2-785-3929 (KM DATA INC.)
South East Asia +65-6563-2082 (Unidux Electronics Pte Ltd.)
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Europe +44-1256-811761 (Ashling Microsystems Limited)
Korea +82-2-785-3117 (KM DATA INC.)
South East Asia +65-6569-4661 (Unidux Electronics Pte Ltd.)
Website: http://www.ydc.co.jp/micom/index_E.htm

Flash Burner Forward FL-S01, Flash Gang Forward FL-G01

[Manufacturer] Forward Electric Co., Ltd. (Hong Kong)

[Distributor] Application Co., Ltd.

[Target Devices] V850/SB1(70F3033A), V850E/MA1

[Features]

◆Host machine interface supports USB.
◆Easy operation and rich array of GUI software provided
◆Low cost from development to mass production
◆Compact and easy to carry (FL-S01)
◆Gang programmer enabling simultaneous programming of up to 8 devices (FL-G01)
◆Can be used on standalone basis using compact flash (FL-G01).
◆Programming adapter board (option) usable in common for FL-S01 and FL-G01.

[Additional Details]

TEL : +81-42-732-1377 FAX : +81-42-732-1378
Website:http://www.apply.co.jp/index_eng.html

FL-S01

FL-G01

Low-End Lineup (1/2)

Item		V850ES/KE1		V850ES/KF1			
Part No.		μPD703207/3207Y	μPD70F3207H/F3207HY	μPD703208/3208Y	μPD703209/3209Y	μPD703210/3210Y μPD70F3210/F3210Y μPD70F3210H/F3210HY	μPD703211/3211Y μPD70F3211H/F3211HY
CPU core		V850ES		V850ES			
CPU performance		29 MIPS (@20 MHz: 5 MHz × 4)		29 MIPS (@20 MHz: 5 MHz × 4)			
Internal ROM		128 KB (mask)	128 KB (flash)	64 KB (mask)	96 KB (mask)	128 KB (mask) 128 KB (flash)	256 KB (mask) 256 KB (flash)
Internal RAM		4 KB		4 KB		6 KB	12 KB
External bus interface	Bus type	–		Multiplexed			
	Address bus	–		16 bits			
	Data bus	–		8/16 bits			
	Chip select signal	–		2			
Memory controller		–		SDRAM, etc.			
Interrupt sources	Internal	25 (Y products: 26)		25 (Y products: 26)			28 (Y products: 29)
	External	8 (8)Note 1		8(8)Note 1			
Timer/counter		16-bit timer/event counter (TM0) × 1 ch 16-bit timer/event counter (TMP) × 1 ch 8-bit timer/event counter (TMH) × 2 ch 8-bit timer/event counter (TM5) × 2 ch 8-bit interval timer (BRG) × 1 ch		16-bit timer/event counter (TM0) × 2 ch 16-bit timer/event counter (TMP) × 1 chNote 3 8-bit timer/event counter (TMH) × 2 ch 8-bit timer/event counter (TM5) × 2 ch 8-bit interval timer (BRG) × 1 ch			
Watchdog timer		2 ch		2 ch			
Serial interface		CSI × 2 ch UART × 2 ch I²C×1 chNote 2		CSI with automatic transfer function (32-byte buffer) × 1 ch CSI × 2 ch UART × 2 ch I²C × 1 chNote 2			
A/D converter		10-bit×8 ch		10 bits × 8 ch			
D/A converter		–		–			
DMA controller		–		–			
Ports	I/O	43		59			
	Input	8		8			
Debug control unit		–		–			
Other peripheral functions		Watch timer: 1 ch, ROM correction function: 4 points, real-time output		Watch timer: 1 ch, ROM correction function: 4 points, real-time output			
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz			
Power supply voltage		2.7 to 5.5 V		2.7 to 5.5 V			
Power consumption (Typ.)		200 mW (128 KB mask products: 20 MHz @5 V operation) 39.6 mW (128 KB mask products: 10 MHz @3.3 V operation)		150 mW (128 KB mask products: 20 MHz @5 V operation) 29.7 mW (128 KB mask products: 10 MHz @3.3 V operation)			
Package		64-pin TQFP (12 × 12 mm) 64-pin LQFP (10 × 10 mm)		80-pin TQFP (12 × 12 mm) 80-pin QFP (14 × 14 mm)			
Operating ambient temperature		-40 to +85°C		-40 to +85°C			

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.
3. μPD703211, 703211Y, 70F3211H, 70F3211HY only

Item		V850ES/KG1				V850ES/KJ1		
Part No.		μPD703212/3212Y	μPD703213/3213Y	μPD703214/3214Y μPD70F3214/F3214Y μPD70F3214H/F3214HY	μPD703215/3215Y μPD70F3215H/F3215HY	μPD703216/3216Y	μPD703217/3217Y μPD70F3217/F3217Y μPD70F3217H/F3217HY	μPD70F3218H/F3218HY
CPU core		V850ES				V850ES		
CPU performance		29 MIPS (@ 20 MHz: 5 MHz × 4)				29 MIPS (@ 20 MHz: 5 MHz × 4)		
Internal ROM		64 KB (mask)	96 KB (mask)	128 KB (mask) 128 KB (flash)	256 KB (mask) 256 KB (flash)	96 KB (mask)	128 KB (mask) 128 KB (flash)	256 KB (flash)
Internal RAM		4 KB		6 KB	16 KB	6 KB		16 KB
External bus interface	Bus type	Multiplexed/separate				Multiplexed/separate		
	Address bus	22 bits				24 bits		
	Data bus	8/16 bits				8/16 bits		
	Chip select signal	2				4		
Memory controller		SRAM, etc.				SRAM, etc.		
Interrupt sources	Internal	30 (Y products : 31)			33 (Y products : 34)	38(Y products : 40)		41(Y products : 43)
	External	8(8)Note 1				8(8)Note 1		
Timer/counter		16-bit timer/event counter (TM0) × 4 ch 16-bit timer/event counter (TMP) × 1 chNote 2 8-bit timer/event counter (TMH) × 2 ch 8-bit timer/event counter (TM5) × 2 ch 8-bit interval timer (BRG) × 1 ch				16-bit timer/event counter (TM0) × 6 ch 16-bit timer/event counter (TMP) × 1 chNote 3 8-bit timer/event counter (TMH) × 2 ch 8-bit timer/event counter (TM5) × 2 ch 8-bit interval timer (BRG) × 1 ch		
Watchdog timer		2ch				2 ch		
Serial interface		CSI with automatic transfer function (32-byte buffer) × 2 ch CSI × 2 ch UART × 2 ch I²C × 1 chNote 4				CSI with automatic transfer function (32-byte buffer) × 2 ch CSI × 3 ch UART/I²C × 1 chNote 4 UART × 2 ch I²C × 1 chNote 4		
A/D converter		10-bit × 8 ch				10-bit × 16 ch		
D/A converter		8-bit × 2 ch				8-bit × 2 ch		
DMA controller		–				–		
Ports	I/O	76				112		
	Input	8				16		
Debug control unit		–				–		Provided(RUN/break)
Other peripheral functions		Watch timer: 1 ch, ROM correction function: 4 points, real-time output				Watch timer: 1 ch, ROM correction function: 4 points, real-time output		
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz				When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz		
Power supply voltage		2.7 V to 5.5 V				2.7 V to 5.5 V		
Power consumption (Typ.)		150 mW (128 KB mask products: 20 MHz @ 5 V operation) 29.7 mW (128 KB mask products: 10 MHz @ 3.3 V operation)				150 mW (128 KB mask products: 20 MHz @ 5 V operation) 29.7 mW (128 KB mask products: 10 MHz @ 3.3 V operation)		
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)				144-pin LQFP (20 × 20 mm)		
Operating ambient temperature		-40 to +85°C				-40 to +85°C		

Notes 1. Number of external interrupts that can be used to release STOP mode
2. μPD703215, 703215Y, 70F3215H, 70F3215HY only
3. μPD70F3218H, 70F3218HY only
4. Only Y products have an on-chip I²C interface.

Low-End Lineup (2/2)

Item		V850ES/KE1+		V850ES/KF1+	
Part No.		μPD703302/3302Y	μPD70F3302/F3302Y	μPD70F3306/F3306Y	μPD703308/3308Y μPD70F3308/F3308Y
CPU core		V850ES		V850ES	
CPU performance		29 MIPS (@20 MHz: 5 MHz × 4)		29 MIPS (@20 MHz: 5 MHz × 4)	
Internal ROM		128 KB (mask)	128 KB (flash)	128 KB (flash)	256 KB (mask) 256 KB (flash)
Internal RAM		4 KB		6 KB	12 KB
External bus interface	Bus type	–		Multiplexed	
	Address bus	–		16 bits	
	Data bus	–		8/16 bits	
	Chip select signal	–		2	
Memory controller		–		SRAM, etc.	
Interrupt sources	Internal	26 (Y products: 27)		29 (Y products: 30)	
	External	9(9)Note 1		9(9)Note 1	
Timer/counter		16-bit timer/event counter (TM0) × 1 ch 16-bit timer/event counter (TMP) × 1 ch 8-bit timer (TMH) × 2 ch, 8-bit timer/event counter (TM5) × 2 ch, 8-bit interval timer (BRG) × 1 ch		16-bit timer/event counter (TM0) × 2 ch 16-bit timer/event counter (TMP) × 1 ch 8-bit timer (TMH) × 2 ch, 8-bit timer/event counter (TM5) × 2 ch, 8-bit interval timer (BRG) × 1 ch	
Watchdog timer		2 ch		2 ch	
Serial interface		CSI × 2ch UART × 1ch UART (LIN compatible) × 1 ch I²C × 1 chNote 2		CSI with automatic transfer function (32-byte buffer) × 1 ch CSI × 2 ch UART × 1 ch UART (LIN compatible) × 1 ch I²C × 1 chNote 2	
A/D converter		10-bit × 8 ch		10-bit × 8 ch	
D/A converter		–		–	
DMA controller		–		–	
Ports	I/O	43		59	
	Input	8		8	
Debug control unit		–		–	
Other peripheral functions		Watch timer: 1 ch, ROM correction function: 4 points, POC/LVI/clock monitor, real-time output		Watch timer: 1 ch, ROM correction function: 4 points, POC/LVI/clock monitor, real-time output	
Operating frequency		Using main clock: 2 to 20 MHz Using subclock: 32.768 kHz Ring-OSC: 240 kHz		Using main clock: 2 to 20 MHz Using subclock: 32.768 kHz Ring-OSC: 240 kHz	
Power supply voltage		2.7 to 5.5V		2.7 to 5.5V	
Power consumption (Typ.)		200 mW (128 KB mask products: 20 MHz @ 5 V operation) 39.6 mW (128 KB mask products: 10 MHz @ 3.3 V operation)		220 mW (256 KB mask products: 20 MHz @ 5 V operation) 42.9 mW (256 KB mask products: 10 MHz @ 3.3 V operation)	
Package		64-pin TQFP (12 × 12 mm) 64-pin LQFP (10 × 10 mm)		80-pin TQFP (12 × 12 mm) 80-pin QFP (14 × 14 mm)	
Operating ambient temperature		-40°C to +85°C		-40°C to +85°C	

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

Item		V850ES/KG1+		V850ES/KJ1+	
Part No.		μPD70F3311/F3311Y	μPD703313/3313Y μPD70F3313/F3313Y	μPD70F3316/F3316Y	μPD70F3318/F3318Y
CPU core		V850ES		V850ES	
CPU performance		29 MIPS (@ 20 MHz : 5 MHz × 4)		29 MIPS (@ 20 MHz : 5 MHz × 4)	
Internal ROM		128 KB (flash)	256 KB (mask) 256 KB (flash)	128 KB (flash)	256 KB (flash)
Internal RAM		6 KB	16 KB	6 KB	16 KB
External bus interface	Bus type	Multiplexed/separate		Multiplexed/separate	
	Address bus	22 bits		24 bits	
	Data bus	8/16 bits		8/16 bits	
	Chip select signal	2		4	
Memory controller		SRAM, etc.		SRAM, etc.	
Interrupt sources	Internal	41 (Y products: 42)		46 (Y products: 48)	
	External	9 (9)Note 1		9 (9)Note 1	
Timer/counter		16-bit timer/event counter (TM0) × 4 ch 16-bit timer/event counter (TMP) × 1 ch 8-bit timer (TMH) × 2 ch, 8-bit timer/event counter (TM5) × 2 ch, 8-bit interval timer (BRG) × 1 ch		16-bit timer/event counter (TM0) × 6 ch 16-bit timer/event counter (TMP) × 1 ch 8-bit timer (TMH) × 2 ch, 8-bit timer/event counter (TM5) × 2 ch, 8-bit interval timer (BRG) × 1 ch	
Watchdog timer		2ch		2ch	
Serial interface		CSI with automatic transfer function (32-byte buffer) × 2 ch CSI × 1 ch UART/CSI × 1 ch UART × 1 ch UART (LIN compatible) × 1 ch I²C × 1 chNote 2		CSI with automatic transfer function (32-byte buffer) × 2 ch CSI × 2 ch UARTNote3/CSI × 1 ch UARTNote3/I²C × 1 chNote2 UART (LIN compatible) × 1 ch UART× 1 ch, I²C × 1 chNote 2	
A/D converter		10-bit × 8 ch		10-bit × 16 ch	
D/A converter		8-bit × 2 ch		8-bit × 2 ch	
DMA controller		4 ch		4 ch	
Ports	I/O	76		112	
	Input	8		16	
Debug control unit		–		–	Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch, ROM correction function: 4 points, POC/LVI/clock monitor, real-time output		Watch timer: 1 ch, POC/LVI/clock monitor, real-time output	
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz Ring-OSC: 240 kHz		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz Ring-OSC: 240 kHz	
Power supply voltage		2.7 to 5.5 V		2.7 to 5.5 V	
Power consumption (Typ.)		220 mW (256 KB mask products: 20 MHz @ 5 V operation) 42.9 mW (256 KB mask products: 10 MHz @ 3.3 V operation)		275 mW (256 KB flash products: 20 MHz @ 5 V operation) 59.4 mW (256 KB flash products: 10 MHz @ 3.3 V operation)	
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)		144-pin LQFP (20 × 20 mm)	
Operating ambient temperature		-40°C to +85°C		-40°C to +85°C	

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.
3. These UARTs are the identical and the number of channels in KJ1+ totals 3 channels.

Middle-Range Lineup (1/3)

Item		V850ES/SG2					
Part No.	Without IEBus, aFCAN	μPD703260/3260Y	μPD703261/3261Y	μPD70F3261/F3261Y	μPD703262/3262Y	μPD703263/3263Y	μPD70F3263/F3263Y
	On-chip IEBus	μPD703270/3270Y	μPD703271/3271Y	μPD70F3271/F3271Y	μPD703272/3272Y	μPD703273/3273Y	μPD70F3273/F3273Y
	On-chip aFCAN	μPD703280/3280Y	μPD703281/3281Y	μPD70F3281/F3281Y	μPD703282/3282Y	μPD703283/3283Y	μPD70F3283/F3283Y
CPU core		V850ES					
CPU performance		29 MIPS (@ 20 MHz)					
Internal ROM		256 KB (mask)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		24 KB	32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate					
	Address bus	22 bits					
	Data bus	8/16 bits					
	Chip select signal	–					
Memory controller		SRAM, etc.					
Interrupt sources	Internal	47[Note 1]/52[Note 2]					
	External	9(9)[Note 1]					
Timer/counter		16-bit interval timer(TMM) × 1 ch 16-bit timer/event counter(TMP) × 6 ch 16-bit timer/event counter(TMQ) × 1 ch					
Watchdog timer		1 ch					
Serial interface		CSI × 3 ch UART(LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch[Note 4] UART(LIN compatible)/I²C × 2 ch[Note 4]					
A/D converter		10-bit × 12 ch					
D/A converter		8-bit × 2 ch					
DMA controller		4 ch					
Ports	I/O	84					
	Input	–					
Debug control unit		–		Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch IEBus controller × 1 ch[Note 5] aFCAN controller × 1 ch[Note 6] ROM correction function : 4 points Real-time output LVI/clock monitor					
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz Ring-OSC: 200 kHz					
Power supply voltage		2.85 to 3.6 V (@ 20 MHz)					
Power consumption (Typ.)		59.4 mW(3.3 V,@ 20 MHz)		82.5 mW(3.3 V,@ 20 MHz)	59.4 mW(3.3 V,@ 20 MHz)		89.1 mW(3.3 V,@ 20 MHz)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)					
Operating ambient temperature		-40°C to +85°C					

Notes1.Only products without IEBus or aFCAN
2.Only products with IEBus or aFCAN
3.Number of external interrupts that can be used to release STOP mode

Notes4.Only Y products have an on-chip I²C interface.
5.μPD703270 (Y)/3271 (Y)/F3271 (Y)/3272 (Y)/3273 (Y)/F3273 (Y)
6.μPD703280 (Y)/3281 (Y)/F3281 (Y)/3282 (Y)/3283 (Y)/F3283 (Y)

Item		V850ES/SG2					
Part No.	Without IEBus, aFCAN	μPD703260/3260Y	μPD703261/3261Y	μPD70F3261/F3261Y	μPD703262/3262Y	μPD703263/3263Y	μPD70F3263/F3263Y
	On-chip IEBus	μPD703270/3270Y	μPD703271/3271Y	μPD70F3271/F3271Y	μPD703272/3272Y	μPD703273/3273Y	μPD70F3273/F3273Y
	On-chip aFCAN	μPD703280/3280Y	μPD703281/3281Y	μPD70F3281/F3281Y	μPD703282/3282Y	μPD703283/3283Y	μPD70F3283/F3283Y
CPU core		V850ES					
CPU performance		29 MIPS (@ 20 MHz)					
Internal ROM		256 KB (mask)	384 KB (mask)	384 KB (flash)	512 KB (mask)	640 KB (mask)	640 KB (flash)
Internal RAM		24 KB	32 KB		40 KB	48 KB	
External bus interface	Bus type	Multiplexed/separate					
	Address bus	22 bits					
	Data bus	8/16 bits					
	Chip select signal	–					
Memory controller		SRAM, etc.					
Interrupt sources	Internal	47[Note 1]/52[Note 2]					
	External	9(9)[Note 1]					
Timer/counter		16-bit interval timer(TMM) × 1 ch 16-bit timer/event counter(TMP) × 6 ch 16-bit timer/event counter(TMQ) × 1 ch					
Watchdog timer		1 ch					
Serial interface		CSI × 3 ch UART(LIN compatible)/CSI × 1 ch CSI/I²C × 1 ch[Note 4] UART(LIN compatible)/I²C × 2 ch[Note 4]					
A/D converter		10-bit × 12 ch					
D/A converter		8-bit × 2 ch					
DMA controller		4 ch					
Ports	I/O	84					
	Input	–					
Debug control unit		–		Provided (RUN/break)	–		Provided (RUN/break)
Other peripheral functions		Watch timer: 1 ch IEBus controller × 1 ch[Note 5] aFCAN controller × 1 ch[Note 6] ROM correction function : 4 points Real-time output LVI/clock monitor					
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz Ring-OSC: 200 kHz					
Power supply voltage		2.85 to 3.6 V (@ 20 MHz)					
Power consumption (Typ.)		59.4 mW(3.3 V,@ 20 MHz)		82.5 mW(3.3 V,@ 20 MHz)	59.4 mW(3.3 V,@ 20 MHz)		89.1 mW(3.3 V,@ 20 MHz)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)					
Operating ambient temperature		-40°C to +85°C					

Notes 1. Only products without IEBus or aFCAN
2. Only products with IEBus or aFCAN
3. Only products with two aFCAN channels
4. Number of external interrupts that can be used to release STOP mode

Notes 5. Only Y products have an on-chip I²C interface.
6. μPD703274(Y)/F3274(Y)/3275(Y)/3276(Y)/F3276(Y)
7. μPD703284(Y)/F3284(Y)/3285(Y)/3286(Y)/F3286(Y)
8. μPD703287(Y)/3288(Y)/F3288(Y)

Middle-Range Lineup (2/3)

Item		V850/SB1						
Part No.		μPD703031B/3031BY	μPD703033B/3033BY	μPD70F3033B/F3033BY	μPD703030B/3030BY	μPD70F3030B/F3030BY	μPD703032B/3032BY	μPD70F3032B/F3032BY
CPU core		V850						
CPU performance		23 MIPS (@20 MHz)						
Internal ROM		128 KB (mask)	256 KB (mask)	256 KB (flash)	384 KB (mask)	384 KB (flash)	512 KB (mask)	512 KB (flash)
Internal RAM		8 KB	16 KB		24 KB			
External bus interface	Bus type	Multiplexed/separate						
	Address bus	22 bits						
	Data bus	16 bits						
	Chip select signal	–						
Memory controller		SRAM, etc.						
Interrupt sources	Internal	31 (Y products: 32)						
	External	8(6)Note 1						
Timer/counter		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 6 ch 8-bit timer × 2 ch						
Watchdog timer		1 ch						
Serial interface		CSI × 1 ch CSI/I²C × 2 chNote 2 CSI/UART × 2 ch						
A/D converter		10-bit × 12 ch						
D/A converter		–						
DMA controller		6 ch (dedicated internal RAM←→on-clip peripheral I/O)						
Ports	I/O	71						
	Input	12						
Debug control unit		–						
Other peripheral functions		ROM correction function:4 points, watch timer: 1 ch						
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz						
Power supply voltage		4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)						
Power consumption (Typ.)		125 mW (5 V, @ 20 MHz)		165 mW (5 V, @ 20 MHz)	125 mW (5 V, @ 20 MHz)	185 mW (5 V, @ 20 MHz)	125 mW (5 V, @ 20 MHz)	210 mW (5 V, @ 20 MHz)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)					100-pin QFP (14 × 20 mm)	
Operating ambient temperature		-40 to +85°C						

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

Item		μPD703229Y		V850/SC1	V850/SC2	V850/SC3		V850/SC1,V850/SC2,V850/SC3
Part No.		μPD703229Y	μPD70F3229Y	μPD703068Y	μPD703069Y	μPD703088Y	μPD703089Y	μPD70F3089Y
CPU core		V850ES		V850				
CPU performance		29 MIPS (@ 20 MHz)		23 MIPS (@ 20 MHz)	21 MIPS (@ 19 MHz)	18 MIPS (@ 16 MHz)		23 MIPS (@ 20 MHz)
Internal ROM		384 KB (mask)	384 KB (flash)	512 KB (mask)				512 KB (flash)
Internal RAM		32 KB		24 KB				
External bus interface	Bus type	Multiplexed		Multiplexed (can be separated only for V850/SC1, V850/SC2)				
	Address bus	18 bits		22 bits				
	Data bus	8/16 bits		16 bits				
	Chip select signal	2		–				
Memory controller		SRAM, etc.		SRAM, etc.				
Interrupt sources	Internal	38 sources		42	44	46	49	
	External	9 (9)Note		11 (9)Note				
Timer/counter		16-bit internal timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 1 ch		16-bit timer/event counter × 10 ch				
Watchdog timer		1 ch		1ch				
Serial interface		UART (LIN compatible) × 3 ch CSI × 1 ch CSI/I²C × 1 ch		CSI × 2 ch CSI/I²C × 2 ch CSI/UART × 2 ch UART × 2 ch				
A/D converter		10-bit × 12 ch		10-bit × 12 ch				
D/A converter		–		–				
DMA controller		4 ch		6 ch (dedicated internal RAM←→on-chip peripheral I/O)				
Ports	I/O	84		112				
	Input	–		12				
Debug control unit		–	Provided (RUN, break)	–				
Other peripheral functions		ROM correction function : 4 points, watch timer: 1 ch, LVI/clock monitor		ROM correction function : 4 points, watch timer: 1 ch, IEBus controller : 1 ch (V850/SC2 only), FCAN controller : 2 ch (1 ch : μPD703088Y only) (V850/SC3 only)				
Operating frequency		When using main clock: 2.5 to 20 MHz When using subclock: 32.768 kHz During Ring OSC operation: 200 kHz		When using main clock: 4 to 20 MHz (@5 V)	When using main clock: 4 to 19 MHz (@5 V)	When using main clock: 4 to 16 MHz (@5 V)		When using main clock: 4 to 20 MHz (@5 V)
				When using subclock: 32.768 kHz	When using subclock: 32.768 kHz	When using subclock: 32.768 kHz		When using subclock: 32.768 kHz
Power supply voltage		3.5 to 5.5V		3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)				4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)
Power consumption (Typ.)		100 mW (5 V, @ 20MHz)	145 mW (5 V, @ 20MHz)	125 mW (5 V, @ 20 MHz)	120 mW (5 V, @ 19 MHz)	110 mW (5 V, @ 16 MHz)		150 mW (5 V, @ 20 MHz)
Package		100-pin LQFP (14 × 14 mm)		144-pin LQFP (20 × 20 mm)				
Operating ambient temperature		-40°C to +85°C		-40 to +85°C				

Note Number of external interrupts that can be used to release STOP mode

Middle-Range Lineup (3/3)

Item		V850ES/SA2			V850ES/SA3		V850ES/ST2
Part No.		μPD703200/3200Y	μPD703201/3201Y	μPD70F3201/F3201Y	μPD703204/3204Y	μPD70F3204/F3204Y	μPD703220
CPU core		V850ES					V850ES
CPU performance		29 MIPS (@ 20 MHz)					–
Internal ROM		128 KB (mask)	256 KB (mask)	256 KB (flash)	256 KB (mask)	256 KB (flash)	ROM-less
Internal RAM		8 KB	16 KB				48 KB
External bus interface	Bus type	Multiplexed/separate					Separate/multiplexed (selectable only for CS1)
	Address bus	22 bits			24 bits		22 bits
	Data bus	8/16 bits					8/16 bits
	Chip select signal	4					4
Memory controller		SRAM, etc.					SRAM, etc.
Interrupt sources	Internal	30 (Y products: 31)			31 (Y products: 32)		28
	External	8 (8)[Note1]					9
Timer/counter		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch					16-bit interval timer (TMM) × 1 ch 16-bit timer/event counter (TMP) × 6 ch
Watchdog timer		1 ch					1 ch
Serial interface		CSI × 2 ch			CSI × 3 ch		CSI × 1 ch CSI/UART × 1 ch UART × 1 ch
		CSI/UART × 1 ch CSI/I²C × 1 ch[Note 2] UART × 1 ch					
A/D converter		10-bit × 12 ch			10-bit × 16 ch		10-bit × 8 ch
D/A converter		8-bit × 2 ch					8-bit × 2 ch
DMA controller		4 ch					–
Ports	I/O	68			84		57
	Input	14			18		8
Debug control unit		–					–
Other peripheral functions		ROM correction function : 4 points, real-time counter (watch timer): 1 ch					Real-time output
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz					20 to 34 MHz
Power supply voltage		2.2 to 2.7 V					3.0 to 3.6 V
Power consumption (Typ.)		38 mW (2.5 V, @ 20 MHz)		46 mW (2.5 V, @ 20 MHz)	38 mW (2.5 V, @ 20 MHz)	46 mW (2.5 V, @ 20 MHz)	T.B.D.
Package		100-pin TQFP (14 × 14 mm)			121-pin FBGA (12 × 12 mm)		120-pin TQFP (14 × 14 mm) 144-pin LQFP (20 × 20 mm)
Operating ambient temperature		-40°C to +85°C					-40°C to +85°C

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

Item		V850/SA1						
Part No.		μPD703014A/3014AY	μPD703014B/3014BY	μPD703015A/3015AY	μPD703015B/3015BY	μPD70F3015B/F3015BY	μPD703017A/3017AY	μPD70F3017A/F3017AY
CPU core		V850						
CPU performance		23 MIPS (@ 20 MHz)						
Internal ROM		64 KB (mask)		128 KB (mask)		128 KB (flush)	256 KB (mask)	256 KB (flash)
Internal RAM		4 KB					8 KB	
External bus interface	Bus type	Multiplexed/separate						
	Address bus	22 bits						
	Data bus	16 bits						
	Chip select signal	–						
Memory controller		SRAM, etc.						
Interrupt sources	Internal	24						
	External	8 (5)[Note 1]						
Timer/counter		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch						
Watchdog timer		1ch						
Serial interface		CSI × 1 ch, CSI/I²C × 1 ch[Note 2] CSI/UART × 1 ch UART × 1ch						
A/D converter		10-bit × 12 ch						
D/A converter		–						
DMA controller		3 ch (dedicated internal RAM←→on-chip peripheral I/O)						
Ports	I/O	72						
	Input	13						
Debug control unit		–						
Other peripheral functions		Watch timer: 1 ch						
Operating frequency		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz						
Power supply voltage		3.0 to 3.6 V (@20 MHz) 2.7 to 3.6 V (@17 MHz)						
Power consumption (Typ.)		66 mW (3.3 V, @ 20 MHz) 56 mW (3.0 V, @ 17 MHz)				105 mW (3.3 V, @ 20 MHz) 99 mW (3.0 V, @ 17 MHz)	66 mW (3.3 V, @ 20 MHz) 56 mW (3.0 V, @ 17 MHz)	105 mW (3.3 V, @ 20 MHz) 99 mW (3.0 V, @ 17 MHz)
Package		121-pin FBGA (12 × 12 mm)	100-pin LQFP (14 × 14 mm)	121-pin FBGA (12 × 12 mm)	100-pin LQFP (14 × 14 mm)		100-pin LQFP (14 × 14 mm) 121-pin FBGA (12 × 12 mm)	
Operating ambient temperature		-40°C to +85°C						

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

ASSP Lineup (1/3)

Item		V850E/IA4			V850E/IA3		V850E/IA1		V850E/IA2	
Part No.		μPD703185	μPD703186	μPD70F3186	μPD703183	μPD70F3184	μPD703116	μPD70F3116	μPD703114	μPD70F3114
CPU core		V850E1			V850E1		V850E1		V850E1	
CPU performance		82 MIPS (@ 64 MHz)			82 MIPS (@ 64 MHz)		67 MIPS (@ 50 MHz)		54 MIPS (@ 40 MHz)	
Internal ROM		128 KB (mask)	256 KB (mask)	256 KB (flash)	128 KB (mask)	256 KB (flash)	256 KB (mask)	256 KB (flash)	128 KB (mask)	128 KB (flash)
Internal RAM		6 KB	12 KB		6 KB	12 KB	10 KB		6 KB	
External bus interface	Bus type	–			–		Multiplexed		Multiplexed	
	Address bus	–			–		24 bits		22 bits	
	Data bus	–			–		8/16 bits		8/16 bits	
	Chip select signal	–			–		8		–	
Memory controller		–			–		SRAM, etc.		SRAM, etc.	
Interrupt sources	Internal	53			49		45		42	
	External	8 (7) Note			7 (6) Note		20(14) Note		16(12) Note	
Timer/counter		16-bit timer/event counter (TMQ) × 2 ch (inverter timer support possible) 16-bit encoder counter/timer (TMENC) × 2 ch 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch			16-bit timer/event counter (TMQ) × 1 ch (inverter timer support possible) 16-bit encoder counter/timer (TMENC) × 1 ch 16-bit timer/event counter (TMP) × 2 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit timer/counter (TMP) × 2 ch 16-bit interval timer (TMM) × 1 ch		16-bit 3-phase sinusoidal PWM timer × 2 ch 16-bit encoder counter/timer × 2 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch		16-bit 3-phase sinusoidal PWM timer × 2 ch 16-bit encoder counter/timer × 1 ch 16-bit timer/counter × 2 ch 16-bit timer/event counter × 1 ch 16-bit interval timer × 1 ch	
Watchdog timer		1 ch			1 ch		–		–	
Serial interface		CSI × 1 ch UART × 1 ch CSI/UART × 1 ch			CSI × 1 ch UART × 1 ch CSI/UART × 1 ch		CSI × 2 ch UART × 3 ch		CSI × 1 ch CSI/UART × 1 ch UART × 1 ch	
A/D converter		10-bit × 4 ch, 2 units (conversion time: 2 μs) 8/10-bit × 8 ch			10-bit × 4 ch, 10-bit × 2 ch (conversion time: 2 μs) 8/10-bit × 6 ch		10-bit × 8 ch, 2 units		10-bit × 6 ch (A/D converter 0) 10-bit × 8 ch (A/D converter 1)	
D/A converter		–			–		–		–	
DMA controller		4 ch			4 ch		4 ch		4 ch	
Ports	I/O	56			44		75		47	
	Input	8			6		8		6	
Debug control unit		-		Provided (RUN/break)	–		–		–	
Other peripheral functions		ROM correction function : 4 points, operational amplifier, comparator, software pull-up function			ROM correction function : 4 points, operational amplifier, comparator, software pull-up function		FCAN controller × 1 ch		–	
Operating frequency		0.5 to 64 MHz			0.5 to 64 MHz		4 to 50 MHz		4 to 40 MHz	
Power supply voltage		2.5 V (internal), 5 V (A/D converter) 5 V (external)			2.5 V (internal), 5 V (A/D converter) 5 V (external)		3.3 V (internal), 5 V (A/D converter) 5 V (external)		5 V (3.3 V (internal), 5 V (A/D converter)) 5 V (external) (on-chip regulator)	
Power consumption (Typ.)		175 mW (internal 2.5 V, @ 64 MHz)			175 mW (internal 2.5 V, @ 64 MHz)		630 mW (internal 3.3 V, external 5 V, @ 50 MHz operation)		440 mW (5 V, @ 40 MHz operation)	
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)			80-pin QFP (14 × 14 mm)		144-pin LQFP (20 × 20 mm)		100-pin QFP (14 × 20 mm) 100-pin LQFP (14 × 14 mm)	
Operating ambient temperature		-40°C to +85°C			-40°C to +85°C		-40°C to +85°C (Provided 110°C products)		-40°C to +85°C	

Note Number of external interrupts that can be used to release STOP mode.

Item		V850ES/IK1		V850/SB2			
Part No.		μPD703327	μPD703329 μPD70F3329	μPD703034B/3034BY	μPD703035B/3035BY μPD70F3035B/F3035BY	μPD703036H/3036HY μPD70F3036H/F3036HY	μPD703037H/3037HY μPD70F3037H/F3037HY
CPU core		V850ES		V850			
CPU performance		41MIPS (@ 32 MHz)		15 MIPS (@ 13 MHz)		22MIPS (@ 19 MHz)	
Internal ROM		64 KB (mask)	128 KB (mask) 128 KB (flash)	128 KB (mask)	256 KB (mask) 256 KB (flash)	384 KB (mask) 384 KB (flash)	512 KB (mask) 512 KB (flash)
Internal RAM		4 KB	6 KB	8 KB	16 KB	24 KB	
External bus interface	Bus type	–		Multiplexed/separate			
	Address bus	–		22 bits			
	Data bus	–		16 bits			
	Chip select signal	–		–			
Memory controller		–		SRAM, etc.			
Interrupt sources	Internal	36		33 (Y products : 34)			
	External	7 (6) Note 1		8 (6) Note 1			
Timer/counter		16-bit timer/event counter (TMQ) × 1ch (inverter timer support possible) 16-bit timer/event counter (TMP) × 1 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit timer counter (TMP) × 3 ch 16-bit interval timer (TMM) × 1 ch		16-bit timer/event counter × 2 ch 8-bit timer/event counter × 4 ch 8-bit timer × 2 ch			
Watchdog timer		1 ch		1 ch			
Serial interface		CSI × 1 ch UART × 2 ch		CSI × 1 ch CSI/I²C × 2 ch Note 2 CSI/UART × 2 ch			
A/D converter		10 bits × 4 ch, 2 units (conversion time 2 μs)		10-bit × 12 ch			
D/A converter		–		–			
DMA controller		–		6 ch (dedicated internal RAM ←→on-chip peripheral I/O)			
Ports	I/O	39		71			
	Input	–		12			
Debug control unit		–		–			
Other peripheral functions		ROM correction function : 4 points, software pull-up function, POC/LVI/clock monitor		ROM correction function : 4 points, watch timer × 1 ch, IEBus controller (simple version) : 1 ch			
Operating frequency		20 to 32 MHz		When using main clock: 2 to 13 MHz (@ 5 V) When using subclock: 32.768 kHz		When using main clock: 2 to 19 MHz (@ 5 V) When using subclock: 32.768 kHz	
Power supply voltage		3.5 to 5.5 V (A/D converter : 4.5 to 5.5 V)		4.0 to 5.5 V (A/D converter : 4.5 to 5.5 V)			
Power consumption (Typ.)		T.B.D.		75 mW (mask ROM version : @ 5 V, 13 MHz) 125 mW (flash memory version : @ 5 V, 13 MHz)		125 mW (mask ROM version : @5 V, 19 MHz) 185 mW (flash memory version : @ 5 V, 19 MHz)	125 mW (mask ROM version : @ 5 V, 19 MHz) 210 mW (flash memory version : @ 5 V, 19 MHz)
Package		64-pin LQFP (14 × 14 mm)		100-pin LQFP (14 × 14mm) 100-pin QFP (14 × 20mm)			100-pin QFP (14 × 20 mm)
Operating ambient temperature		-40°C to +85°C		-40°C to +85°C			

Notes 1. Number of external interrupts that can be used to release STOP mode.
2. Only Y products have an on-chip I²C interface.

ASSP Lineup (2/3)

Item		V850ES/FE2				V850ES/FF2			
Part No.		μPD703230	μPD70F3230	μPD703231	μPD70F3231	μPD703232	μPD70F3232	μPD703233	μPD70F3233
CPU core		V850ES				V850ES			
CPU performance		29 MIPS (@20 MHz)				29 MIPS (@20 MHz)			
Internal ROM		64 KB (mask)	64 KB (flash)	128 KB (mask)	128 KB (flash)	128 KB (mask)	128 KB (flash)	256 KB (mask)	256 KB (flash)
Internal RAM		4 KB		6 KB		6 KB		12 KB	
External bus interface	Bus type	–				–			
	Address bus	–				–			
	Data bus	–				–			
	Chip select signal	–				–			
Memory controller		–				–			
Interrupt sources	Internal	44				44			
	External	9(9)Note				9(9)Note			
Timer/counter		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TQM) × 1 ch 16-bit interval timer (TMM) × 1 ch				16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 1 ch 16-bit interval timer (TMM) × 1 ch			
Watchdog timer		1 ch				1 ch			
Serial interface		CSI × 2 ch UART (LIN compatible) × 2 ch				CSI × 2 ch UART (LIN compatible) × 2 ch			
A/D converter		10-bit × 10 ch				10-bit × 12 ch			
D/A converter		–				–			
DMA controller		–				–			
Ports	I/O	51				67			
	Input	–				–			
Debug control unit		–	Provided (RUN, break)	–	Provided (RUN, break)	–	Provided (RUN, break)	–	Provided (RUN, break)
Other peripheral functions		Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 1 ch				Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 1 ch			
Operating frequency		When using main clock: 16 to 20 MHz				When using main clock: 16 to 20 MHz			
Power supply voltage		4.0 to 5.5V				4.0 to 5.5V			
Power consumption (Typ.)		155 mW (@5.0 V, 20 MHz)	170 mW (@5.0 V, 20 MHz)	155 mW (@5.0 V, 20 MHz)	170 mW (@5.0 V, 20 MHz)	155 mW (@5.0 V, 20 MHz)	170 mW (@5.0 V, 20 MHz)	155 mW (@5.0 V, 20 MHz)	170 mW (@5.0 V, 20 MHz)
Package		64-pin TQFP (10 × 10 mm)				80-pin TQFP (12 × 12mm)			
Operating ambient temperature		-40°C to +85°C, -40°C to +110°C				-40°C to +85°C, -40°C to +110°C			

Note Number of external interrupts that can be used to release STOP mode

Item		V850ES/FG2					V850ES/FJ2		
Part No.		μPD703234	μPD70F3234	μPD703235	μPD70F3235	μPD70F3236	μPD70F3237	μPD70F3238	μPD70F3239
CPU core		V850ES					V850ES		
CPU performance		29 MIPS (@ 20 MHz)					29 MIPS (@ 20 MHz)		
Internal ROM		128 KB (mask)	128 KB (flash)	256 KB (mask)	256 KB (flash)	384 KB (flash)	256 KB (flash)	384 KB (flash)	512 KB (flash)
Internal RAM		6 KB		12 KB		16 KB	12 KB	16 KB	20 KB
External bus interface	Bus type	–					–		Multiplexed
	Address bus	–					–		16 bits
	Data bus	–					–		8/16 bits
	Chip select signal	–					–		4
Memory controller		–					–		SRAM, etc.
Interrupt sources	Internal	62					73		83
	External	12 (12)Note					16 (16)Note		
Timer/counter		16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 2 ch 16-bit interval timer (TMM) × 1 ch					16-bit timer/event counter (TMP) × 4 ch 16-bit timer/event counter (TMQ) × 3 ch 16-bit interval timer (TMM) × 1 ch		
Watchdog timer		1 ch					1ch		
Serial interface		CSI × 2 ch UART (LIN compatible) × 3 ch					CSI × 3 ch UART (LIN compatible) × 3 ch		CSI × 3 ch UART (LIN compatible) × 4 ch
A/D converter		10-bit × 16 ch					10-bit × 24 ch		
D/A converter		–					–		
DMA controller		4 ch					4 ch		
Ports	I/O	84					128		
	Input	–					–		
Debug control unit		–	Provided (RUN, break)	–	Provided (RUN, break)		Provided (RUN, break)		
Other peripheral functions		Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 2 ch					Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag		
							aFCAN controller: 2 ch		aFCAN controller: 4 ch
Operating frequency		When using main clock: 16 to 20 MHz					When using main clock: 16 to 20 MHz		
Power supply voltage		4.0 to 5.5V					4.0 to 5.5V		
Power consumption (Typ.)		155 mW (@ 5.0 V, 20 MHz)	170 mW (@ 5.0 V, 20 MHz)	155 mW (@ 5.0 V, 20 MHz)	170 mW (@ 5.0 V, 20 MHz)		200 mW (@ 5.0 V, 20 MHz)		
Package		100-pin LQFP (14 × 14 mm)					144-pin LQFP (20 × 20 mm)		
Operating ambient temperature		-40°C to +85°C, -40°C to +110°C					-40°C to +85°C, -40°C to +110°C		

Note Number of external interrupts that can be used to release STOP mode

ASSP Lineup (3/3)

Item		V850E/SV2		V850/SV1					
Part No.		μPD703166/3166Y	μPD70F3166/F3166Y	μPD703041/3041Y	μPD703039/3039Y	μPD703040/3040Y	μPD70F3040/F3040Y	μPD703038/3038Y	μPD70F3038/F3038Y
CPU core		V850E1		V850					
CPU performance		55 MIPS (@ 40.5 MHz)		23 MIPS (@ 20 MHz)					
Internal ROM		512 KB (mask)	512 KB (flash)	192 KB (mask)	256 KB (mask)		256 KB (flash)	384 KB (mask)	384 KB (flash)
Internal RAM		24 KB		8 KB		16 KB			
External bus interface	Bus type	Multiplexed/separate		Multiplexed					
	Address bus	26 bits		22 bits					
	Data bus	8/16 bits		16 bits					
	Chip select signal	8		–					
Memory controller		SRAM, etc.		SRAM, etc.					
Interrupt sources	Internal	75 (Y products : 76)		45 (Y products: 46)					
	External	12(12)Note 1		9(6)Note1					
Timer/counter		32-bit timer/event counter × 1 ch 16-bit timer/event counter × 6 ch 16-bit interval timer × 6 ch 8-bit timer/event counter × 12 ch		24-bit timer/event counter × 2 ch 16-bit timer/event counter × 2 ch 8-bit timer/event counter × 8 ch					
Watchdog timer		1 ch		1 ch					
Serial interface		CSI with automatic transfer function × 2 ch CSI × 3 ch UART/CSI × 1 ch UART × 1 ch I²C × 1 chNote 2		CSI × 1 ch CSI/I²C × 2 chNote 2 CSI/UART × 2ch					
A/D converter		10-bit × 24 ch		10-bit × 16 ch					
D/A converter		–		–					
DMA controller		4 ch		6 ch (dedicated internal RAM←→internal peripheral I/O)					
Ports	I/O	171		135					
	Input	24		16					
Debug control unit		Provided (RUN, break)		–					
Other peripheral functions		Boundary scan function, 12- to 16-bit PWM output : 5 ch, real-time output, ROM correction function : 8 points		Watch timer: 1 ch, 12- to 16-bit PWM output : 4 ch, V_{sync}/H_{sync} separator, ROM correction function : 4 points					
Operating frequency		10 to 40.5 MHz		When using main clock: 4 to 20 MHz When using subclock: 32.768 kHz					
Power supply voltage		2.3 to 2.7 V (internal) 2.7 to 3.6 V (external)		3.1 to 3.6 V (@ 20 MHz) 2.7 to 3.6 V (@ 16 MHz)					
Power consumption (Typ.)		134 mW (@ 2.5 V, 40.5 MHz)	159 mW (@ 2.5 V, 40.5 MHz)	82 mW (@ 3.3 V, 20 MHz)			148 mW (@ 3.3 V, 20 MHz)	82 mW (@ 3.3 V, 20 MHz)	148 mW (@ 3.3 V, 20 MHz)
Package		257-pin FBGA (14 × 14 mm)		176-pin LQFP (24 × 24 mm)	176-pin LQFP (24 × 24 mm) 180-pin FBGA (13 × 13 mm)			180-pin FBGA (13 × 13 mm)	
Operating ambient temperature		-10°C to +70°C		-40°C to +85°C					

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

Item		V850/SF1					V850/DB1		V850ES/PM1
Part No.		μPD703075AY	μPD703076AY	μPD703078AY	μPD703079AY	μPD70F3079AY	μPD70F3080	μPD703081	μPD703228
CPU core		V850					V850		V850ES
CPU performance		18 MIPS (@ 16 MHz)					18 MIPS (@ 16 MHz)		29 MIPS (@ 20 MHz)
Internal ROM		128 KB (mask)		256 KB (mask)		256 KB (flash)	128 KB (flash)	128 KB (mask)	128 KB (mask)/ROM-less
Internal RAM		12 KB		16 KB			6 KB		10 KB
External bus interface	Bus type	Multiplexed					–		Separate
	Address bus	22 bits					–		19 bits
	Data bus	16 bits					–		8/16 bits
	Chip select signal	–					–		3
Memory controller		SRAM, etc.					–		SRAM, etc.
Interrupt sources	Internal	35	38	35	38		44	40	28
	External	8 (6)Note					7 (7)Note 1	7 (7)Note 1	4 (4)Note 1
Timer/counter		16-bit timer/event counter × 8 ch					16-bit timer/event counter (TMG) × 1 ch 16-bit timer/event counter (TM0) × 2 ch 8-bit timer/event counter (TM5) × 2 ch		16-bit timer/event counter (TM1) × 6 ch 8-bit timer/event counter (TM2) × 2 ch
Watchdog timer		1 ch					1 ch		1 ch
Serial interface		CSI × 1 ch CSI/I²C × 1 ch CSI/UART × 2 ch					CSI × 3 ch UART × 2 ch		CSI × 2 ch UART × 2ch
A/D converter		10-bit × 12 ch					10-bit × 8 ch		16-bit × 6 ch (12 inputs)
D/A converter		–					–		–
DMA controller		6 ch (dedicated internal RAM ←→ internal peripheral I/O)					–		–
Ports	I/O	72					99 (Including 16 output-only)		68
	Input	12					8		–
Debug control unit		–					–		–
Other peripheral functions		Watch timer: 1 ch FCAN controller : 1 ch ROM correction function : 4 points	Watch timer: 1 ch FCAN controller : 2 ch ROM correction function : 4 points	Watch timer: 1 ch FCAN controller : 1 ch ROM correction function : 4 points	Watch timer: 1 ch FCAN controller : 2 ch ROM correction function : 4 points		Watch timer: 1 ch,16-bit PWM output: 6 ch 8-bit PWM output: 2 ch, meter control PWM: 24 ch DCAN controller: 2 ch	Watch timer: 1 ch, 16-bit PWM output: 6 ch 8-bit PWM output: 2 ch, meter control PWM: 24 ch DCAN controller: 1 ch	Real-time counter (watch timer) : 1 ch ROM correction function : 4 points 8- to 12-bit PWM output : 4 ch
Operating frequency		When using main clock: 4 to 16 MHz When using subclock: 32.768 kHz					When using main clock: 4 to 16 MHz		When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz
Power supply voltage		3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)					4.0 to 5.5 V		3.0 to 3.6 V (@ 20 MHz) 2.7 to 3.6 V (@ 10 MHz) 2.2 to 3.6 V (@ 32.768 kHz)
Power consumption (Typ.)		75 mW (@ 5 V, 16 MHz)				125 mW (@ 5 V, 16 MHz)	180 mW (@ 5 V, 16 MHz)	120 mW (@ 5 V, 16 MHz)	81 mW (@ 3.3 V, 20 MHz)
Package		100-pin LQFP (14 × 14 mm) 100-pin QFP (14 × 20 mm)					128-pin QFP (20 × 20 mm)		100-pin LQFP (14 × 14 mm)
Operating ambient temperature		-40°C to +85°C					-40°C to +85°C		-40°C to +85°C

Note Number of external interrupts that can be used to release STOP mode

High-End Lineup (1/2)

Item		V850E/MA3					V850E/ME2
Part No.		μPD703131A/3131AY	μPD703132A/3132AY	μPD703133A/3133AY	μPD703134A/3134AY	μPD70F3134A/F3134AY	μPD703111A
CPU core		V850E1					V850E1
CPU performance		106 MIPS (@ 80 MHz)					215 MIPS (@ 150 MHz)
Internal ROM		256 KB (mask)		512 KB (mask)		512 KB (flash)	ROM-less (instruction cache : 8 KB)
Internal RAM		16 KB	32 KB	16 KB	32 KB		Instruction: 128 KB; Data: 16 KB
External bus interface	Bus type	Multiplexed/separate					Separate
	Address bus	26 bits					26 bits
	Data bus	8/16 bits					8/16/32 bits
	Chip select signal	8					8
Memory controller		SDRAM, SRAM, etc.					SDRAM, SRAM, etc.
Interrupt sources	Internal	41					59
	External	26(26)Note 1					40(32)Note 1
Timer/counter		16-bit interval timer (TMD) × 4 ch 16-bit timer/event counter (TMP) × 3 ch 16-bit timer/event counter (TMQ) × 1 ch (inverter timer support possible) 16-bit encoder counter/timer (TMENC) × 1 ch					16-bit timer/event counter (TMC) × 6 ch 16-bit interval timer (TMD) × 4 ch 16-bit encoder counter/timer (TMENC) × 2 ch
Watchdog timer		1 ch					–
Serial interface		CSI/UART × 3 ch UART/I²C × 1 chNote 2					CSI (with FIFO) × 1 ch CSI (with FIFO)/UART × 1 ch UART × 1 ch
A/D converter		10-bit × 8 ch					10-bit × 8 ch
D/A converter		8-bit × 2 ch					–
DMA controller		4 ch					4 ch
Ports	I/O	101					77
	Input	11					1
Debug control unit		Provided (RUN, break)					Provided (RUN, break, trace)
Other peripheral functions		ROM correction function : 4 points					USB (function) × 1 ch, SSCG 16-bit PWM output × 2 ch
Operating frequency		5 to 80 MHz					10 to 150 MHz
Power supply voltage		2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)					1.35 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 133 MHz) 1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
Power consumption (Typ.)		T.B.D.				575 mW (@2.5 V, 80 MHz)	200 mW (@ 1.5 V, 150 MHz)
Package		144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)					176-pin LQFP (24 × 24 mm) 240-pin FBGA (16 × 16 mm)
Operating ambient temperature		-40°C to +85°C					-40°C to +85°C (@133MHz), -40 to°C +70°C (@150MHz)

Notes 1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface.

Item		V850E/MA1					V850E/MA2
Part No.		μPD703103A	μPD703105A	μPD703106A	μPD703107A	μPD70F3107A	μPD703108
CPU core		V850E1					V850E1
CPU performance		–	67 MIPS (@ 50 MHz)				–
Internal ROM		ROM-less	128 KB (mask)		256 KB (mask)	256 KB (flash)	ROM-less
Internal RAM		4 KB		10 KB			4 KB
External bus interface	Bus type	Separate					Separate
	Address bus	26 bits					25 bits
	Data bus	8/16 bits					8/16 bits
	Chip select signal	8					4
Memory controller		SDRAM, SRAM, etc.					SDRAM, SRAM, etc.
Interrupt sources	Internal	33					23
	External	25 (17)Note					8 (4)Note
Timer/counter		16-bit timer/event counter (TMC) × 4 ch 16-bit interval timer (TMD) × 4 ch					16-bit timer/event counter (TMC) × 2 ch 16-bit interval timer (TMD) × 4 ch
Watchdog timer		–					–
Serial interface		CSI × 1 ch CSI/UART × 2 ch UART × 1 ch					CSI/UART × 2 ch
A/D converter		10-bit × 8 ch					10-bit × 4 ch
D/A converter		–					–
DMA controller		4 ch					4 ch
Ports	I/O	106					74
	Input	9					5
Debug control unit		–					–
Other peripheral functions		12-bit PWM output × 2ch					–
Operating frequency		4 to 50 MHz					4 to 40 MHz
Power supply voltage		3.0 to 3.6 V					3.0 to 3.6 V
Power consumption (Typ.)		528 mW (@ 3.3 V, 50 MHz)				627 mW (@ 3.3 V, 50 MHz)	416 mW (@ 3.3 V, 40 MHz)
Package		144-pin LQFP (20 × 20 mm)		144-pin LQFP (20 × 20 mm) 161-pin FBGA (13 × 13 mm)			100-pin LQFP (14 × 14 mm)
Operating ambient temperature		-40°C to +85°C					-40°C to +85°C

Note Number of external interrupts that can be used to release STOP mode

High-End Lineup (2/2)

Item		V850E/MS1				V850E/MS2
Part No.	External 3.3V	μPD703100A-33/-40	μPD703101A-33	μPD703102A-33	μPD70F3102A-33	μPD703130
	External 5V	μPD703100-33/-40	μPD703101-33	μPD703102-33	μPD70F3102-33	
CPU core		V850E1				V850E1
CPU performance		–	47 MIPS (@ 33 MHz)			–
Internal ROM		ROM-less	96 KB (mask)	128 KB (mask)	128 KB (flash)	ROM-less
Internal RAM		4 KB				4 KB
External bus interface	Bus type	Separate				Separate
	Address bus	24 bits				24 bits
	Data bus	8/16 bits				8/16 bits
	Chip select signal	8				4
Memory controller		EDO DRAM, SRAM, etc.				EDO DRAM, SRAM, etc.
Interrupt sources	Internal	47				35
	External	25 (1)[Note1]				10 (1)[Note1]
Timer/counter		16-bit timer/event counter × 6 ch 16-bit interval timer × 2 ch				16-bit timer/event counter × 4 ch 16-bit interval timer × 2 ch
Watchdog timer		–				–
Serial interface		CSI × 2 ch CSI/UART × 2 ch				CSI/UART × 2ch
A/D converter		10-bit × 8 ch				10-bit × 4 ch
D/A converter		–				–
DMA controller		4ch				4 ch
Ports	I/O	122				52
	Input	9				5
Debug control unit		–				–
Other peripheral functions		–				–
Operating frequency		2 to 40 MHz (-40 product) 2 to 33 MHz (-33 product)				10 to 33 MHz
Power supply voltage		3.0 to 3.6 V (internal, external) (A products) 3.0 to 3.6 V (internal)/4.5 to 5.5 V (external) (Products without A)				3.0 to 3.6 V (internal)/ 4.5 to 5.5 V (external)
Power consumption (Typ.)		272 mW (@ 3.3 V, 33 MHz) 430 mW (@ 5 V, 33 MHz)			294 mW (@ 3.3 V, 33 MHz) 515 mW (@ 5 V, 33 MHz)	218 mW (@ 3.3 V, 33 MHz)
Package		144-pin LQFP (20 × 20 mm) 157-pin FBGA (14 × 14 mm)[Note2]				100-pin LQFP (14 × 14 mm)
Operating ambient temperature		-40°C to +85°C[Note3]				-40°C to +85°C

Notes 1. Number of external interrupts that can be used to release STOP mode
2. μPD703100A-33, 703101A-33, 703102A-33, and 70F3102A-33 only
3. μPD703100-40, 703100A-40 : -40°C to +70°C
Others : -40°C to +85°C

Item		V853				
Part No.		μPD703003A	μPD703004A	μPD703025A	μPD70F3003A	μPD70F3025A
CPU core		V850				
CPU performance		38 MIPS (@ 33 MHz)				
Internal ROM		128 KB (mask)	96 KB (mask)	256 KB (mask)	128 KB (flash)	256 KB (flash)
Internal RAM		4 KB		8 KB	4 KB	8 KB
External bus interface	Bus type	Multiplexed				
	Address bus	20 bits				
	Data bus	16 bits				
	Chip select signal	–				
Memory controller		SRAM, etc.				
Interrupt sources	Internal	32				
	External	17(1)[Note]				
Timer/counter		16-bit timer/event counter × 4 ch 16-bit interval timer × 1 ch				
Watchdog timer		–				
Serial interface		CSI × 2 ch CSI/UART × 2 ch				
A/D converter		10 bits × 8 ch				
D/A converter		2 ch				
DMA controller		–				
Ports	I/O	67				
	Input	8				
Debug control unit		–				
Other peripheral functions		12-bit PWM output × 2 ch				
Operating frequency		2 to 33 MHz				
Power supply voltage		4.5 to 5.5V				
Power consumption (Typ.)		365 mW (@ 5 V, 33 MHz)		450 mW (@ 5 V, 33 MHz)	425 mW (@ 5 V, 33 MHz)	480 mW (@ 5 V, 33 MHz)
Package		100-pin LQFP (14 × 14 mm)				
Operating ambient temperature		-40°C to +85°C				

Note Number of external interrupts that can be used to release STOP mode

V850 Series Development Environment

The V850 Series development environment consists of tools designed to make the development of application systems using the V850 Series of high-performance microcontrollers made by NEC Electronics more pleasant, faster, and more accurate.

Each one of these development tools features functions to fully exploit the performance of the V850 Series.

Low-Priced Development Environment Lineup

Emulator and evaluation board available at low prices

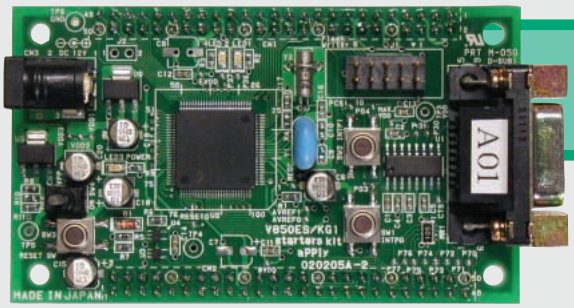
Price

Low-priced full-function emulator IECUBE

- Low prices 1/3 or 1/4 the price of conventional emulators
- Connectable to PC via USB
- Enhanced real-time RAM monitor and time measuring function
- On-chip self-diagnosis function
- Debugger and simple programmer provided
- Palm size

Ultra-low-priced on-chip emulator N-Wire CARD

- Ultra low price 1/10 the price of conventional emulators
- Connectable to PC via PCMCIA
- Writing to the microcontroller on-chip flash memory possible
- Debugger provided



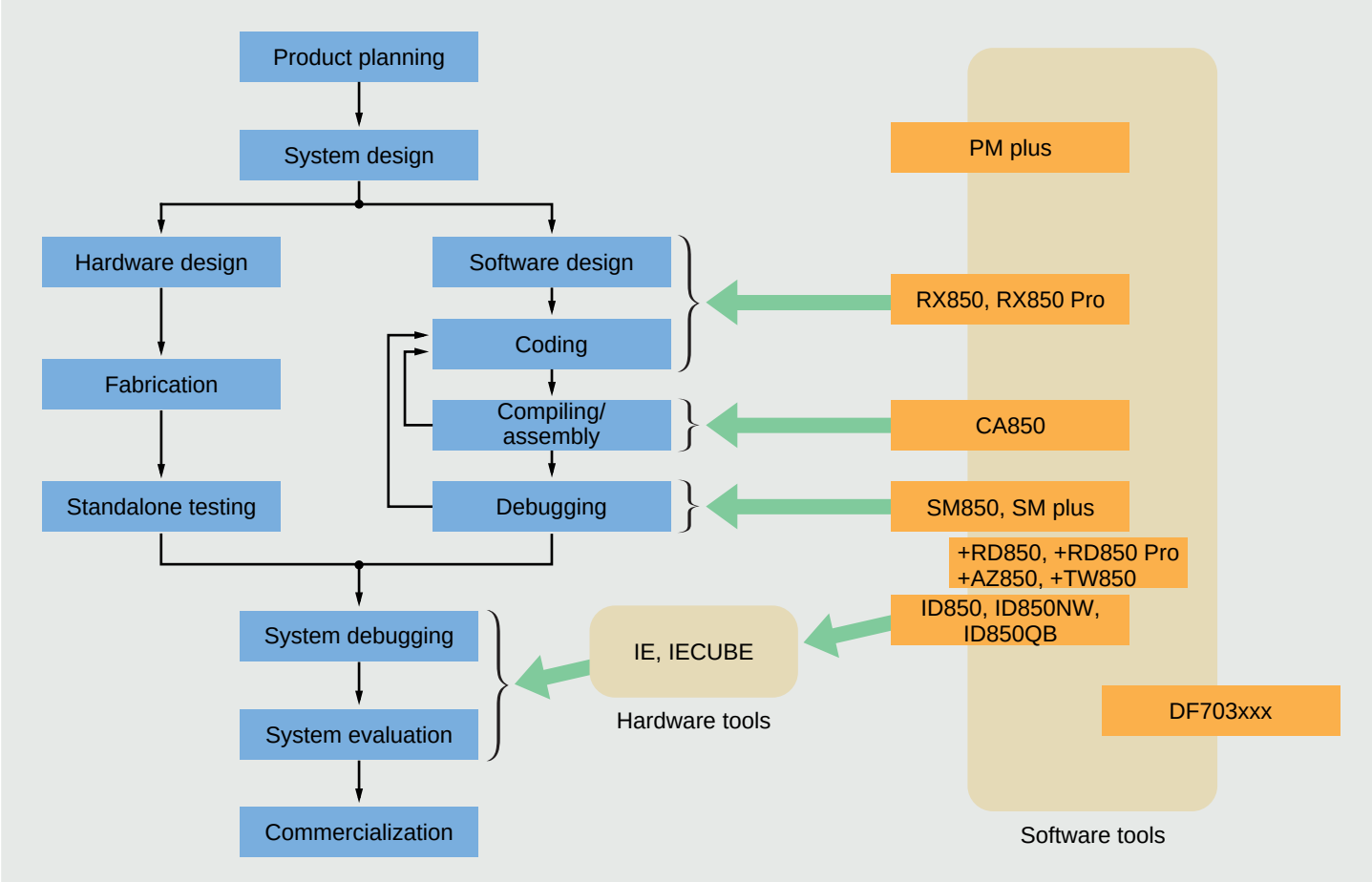
Starter kit for simple evaluation TK-850 Series

- Evaluation kit enabling easy performance testing
- Lineup for V850ES/Kx1, V850ES/SA2, and V850ES/SG2
- Debugger, compiler, and circuit diagrams provided as standard

Function

* For details, refer to V850 Series Development Environment Pamphlet (U15763E)

Development Flow



Development Tools (1/3)

Software tools

Product Name	
Software package	SP850
C compiler	CA850[Note 1]
Device file	DF703xxx[Note 2]
Project Manager	PM plus[Notes 1, 3]
Integrated debugger	ID850[Note 1], ID850NW[Note 1], ID850QB[Note 4]
System simulator	SM850[Note 1], SM plus[Note 5]
Real-time OS	RX850, RX850 Pro
Task debugger	RD850, RD850 Pro[Note 6]
System performance analyzer	AZ850[Note 6]
Middleware	AP703000-Bxxx, AP703100-Bxxx
Performance analysis tool	TW850[Note 1]

Notes 1. Packaged in SP850

2. Download from the NEC Electronics Website.
(URL: http://www.necel.com/micro/index_e.html)

3. Included with CA850

4. Included with IECUBE and IE-V850E1-CD-NW.

5. Instruction simulation version: Included with SP850.
Instruction + peripheral simulation version: Only the SM plus for the μPD70F3261Y is included with SP850.

6. Included with RX850, RX850 Pro

Remark For details, refer to the **V850 Series Development Environment Pamphlet (U15763E)**.

Development Tools (2/3)

Hardware tools (when using IECUBE)

Target Device	In-Circuit Emulator
V850ES/SG2, V850ES/SJ2	QB-V850ESSX2-ZZZ
V850E/IA3, V850E/IA4, V850ES/IK1	QB-V850EIA4-ZZZ
V850ES/KE1, V850ES/KE1+, V850ES/KF1, V850ES/KF1+, V850ES/KG1, V850ES/KG1+, V850ES/KJ1, V850ES/KJ1+	QB-V850ESKX1H-ZZZ
V850ES/FE2, V850ES/FF2, V850ES/FG2, V850ES/FJ2, μPD703229Y, 70F3229Y	QB-V850ESFX2-ZZZ

Remarks 1. A separate socket is required for each above emulator.
2. A power supply, a USB interface cable, a debugger, and a simple programmer are included. A PC interface board is not required.
3. For details, refer to the **V850 Series Development Environment Pamphlet (U15763E).**

Hardware tools (when using N-Wire CARD)

Target Device	On-Chip Debug Emulator
V850E/ME2, V850E/MA3, V850E/IA4, V850E/SV2, V850ES/SG2, V850ES/SJ2, V850ES/FE2, V850ES/FF2, V850ES/FG2, V850ES/FJ2, V850ES/KJ1, V850ES/KJ1+, μPD70F3229Y	IE-V850E1-CD-NW

Remarks 1. A target connection cable, a connector conversion board, a target connector, and a debugger are included. A power supply and a PC interface board are not required.
2. For details, refer to the **V850 Series Development Environment Pamphlet (U15763E).**

Hardware tools (using other emulators)

Target Device	In-Circuit Emulator	
	Main Unit	Emulation Board
V850ES/SA2, V850ES/SA3	IE-V850ES-G1	IE-703204-G1-EM1 Note 1
V850ES/KF1, V850ES/KG1, V850ES/KJ1		IE-703217-G1-EM1 Note 2
V850ES/SG2, V850ES/SJ2		IE-703288-G1-EM1 Note 2
V850ES/PM1		IE-703228-G1-EM1 Note 2
V850ES/FE2, V850/FF2, V850ES/FG2, V850ES/FJ2, μPD703229Y, 70F3229Y		IE-703239-G1-EM1 Note 2
V850ES/ST2		IE-703220-G1-EM1 Note 2
V850E/SV2	IE-V850E-MC-A	IE-703166-MC-EM1
V850E/MA1, V850E/MA2		IE-703107-MC-EM1 Note 3
V850E/IA1	IE-V850E-MC	IE-703116-MC-EM1
V850E/IA2		IE-703114-MC-EM1
V850E/MS1 (5V), V850E/MS2 (5V)	IE-703102-MC	IE-703102-MC-EM1 Note 3
V850E/MS1 (3.3V)		IE-703102-MC-EM1-A
V850/SA1	IE-703002-MC	IE-703017-MC-EM1 Note 3
V850/SB1, V850/SB2		IE-703037-MC-EM1 Note 3
V850/SV1		IE-703040-MC-EM1 Note 3
V850/SF1		IE-703079-MC-EM1 Note 3
V850/SC1, V850/SC2, V850/SC3		IE-703089-MC-EM1
V853		IE-703003-MC-EM1

Notes 1. A separate socket and probe are required for connection to the target system.
The optional PC interface board (IE-70000-PCI-IF-A or IE-70000-CD-IF-A) are required as a common part.
2. A separate socket is required for connection to the target system.
The optional PC interface board (IE-70000-PCI-IF-A or IE-70000-CD-IF-A) are required as a common part.
3. Depending on the target device package, a separate socket and probe may be required.
The following items are required as common items.
- PC interface board: IE-70000-PCI-IF-A or IE-70000-CD-IF-A
- Power supply: IE-70000-MC-PS-B

Remark For details, refer to the **V850 Series Development Environment Pamphlet (U15763E).**

Development Tools (3/3)

●IECUBE configuration example

① In-circuit emulator (IECUBE)
② AC adapter (provided with ①)
③ USB interface cable (provided with ①)
④ Extension probe
⑤ Exchange adapter (provided with ① Note)
⑥ Target connector (provided with ① Note)
⑦ Mount adapter

Note If ordering the in-circuit emulator (①), if the part number ends in "-ZZZ", the above exchange adapter (⑤) and target connector (⑥) are not provided.

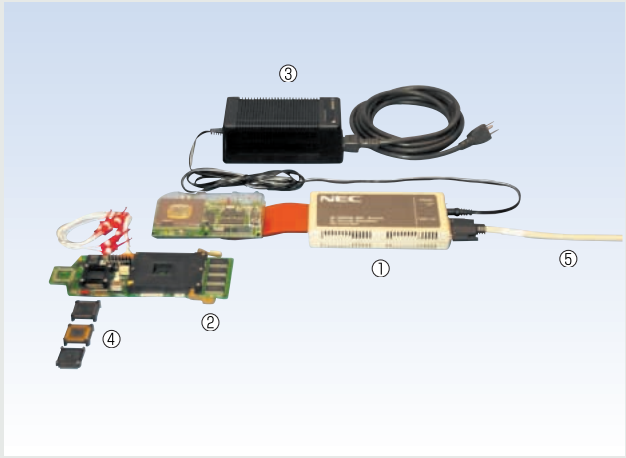
●N-Wire CARD configuration example

① Host machine (with PCMCIA slot)
② On-chip emulator IE-V850E1-CD-NW
③ In-circuit emulator connection cable
④ Connector conversion board
⑤ In-circuit emulator connector

●IE-V850ES-G1 configuration example

① In-circuit emulator (main unit)
② Emulation board (connected inside main unit)
③ Emulation probe
④ Conversion adapter/conversion socket
⑤ PC interface cable (provided with ①)
⑥ Power supply cable (provided with ①)

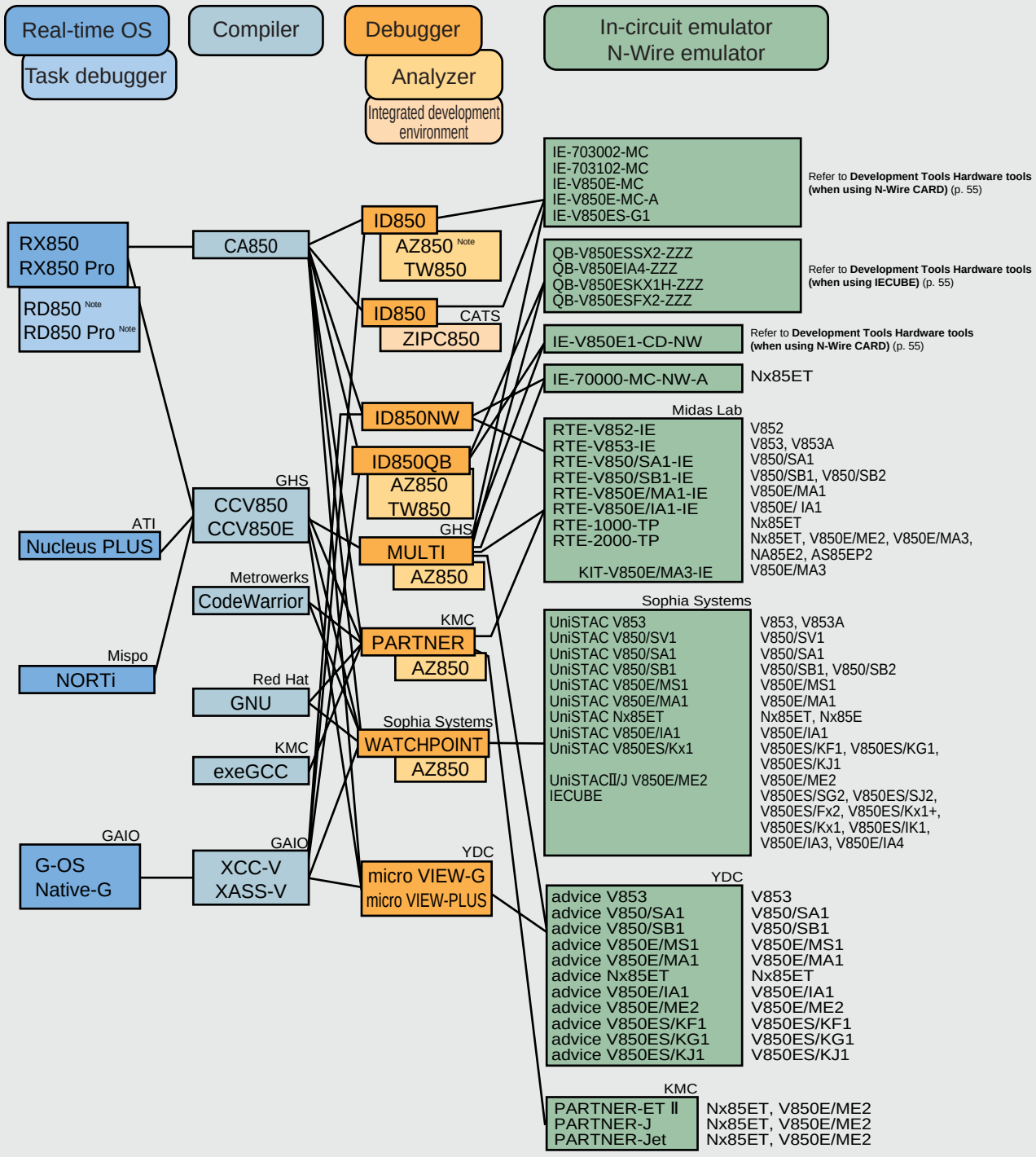
●IE-V850E-MC, IE-V850E-MC-A, IE-703102-MC, IE-703002-MC configuration example



① In-circuit emulator (main unit)
② Option board
③ Power supply unit
④Conversion adapter/conversion socket (provided with ②)
⑤ PC interface cable (provided with ①)

V850 Series Development Environment (1/2)

Development environment using in-circuit emulator, N-Wire emulator

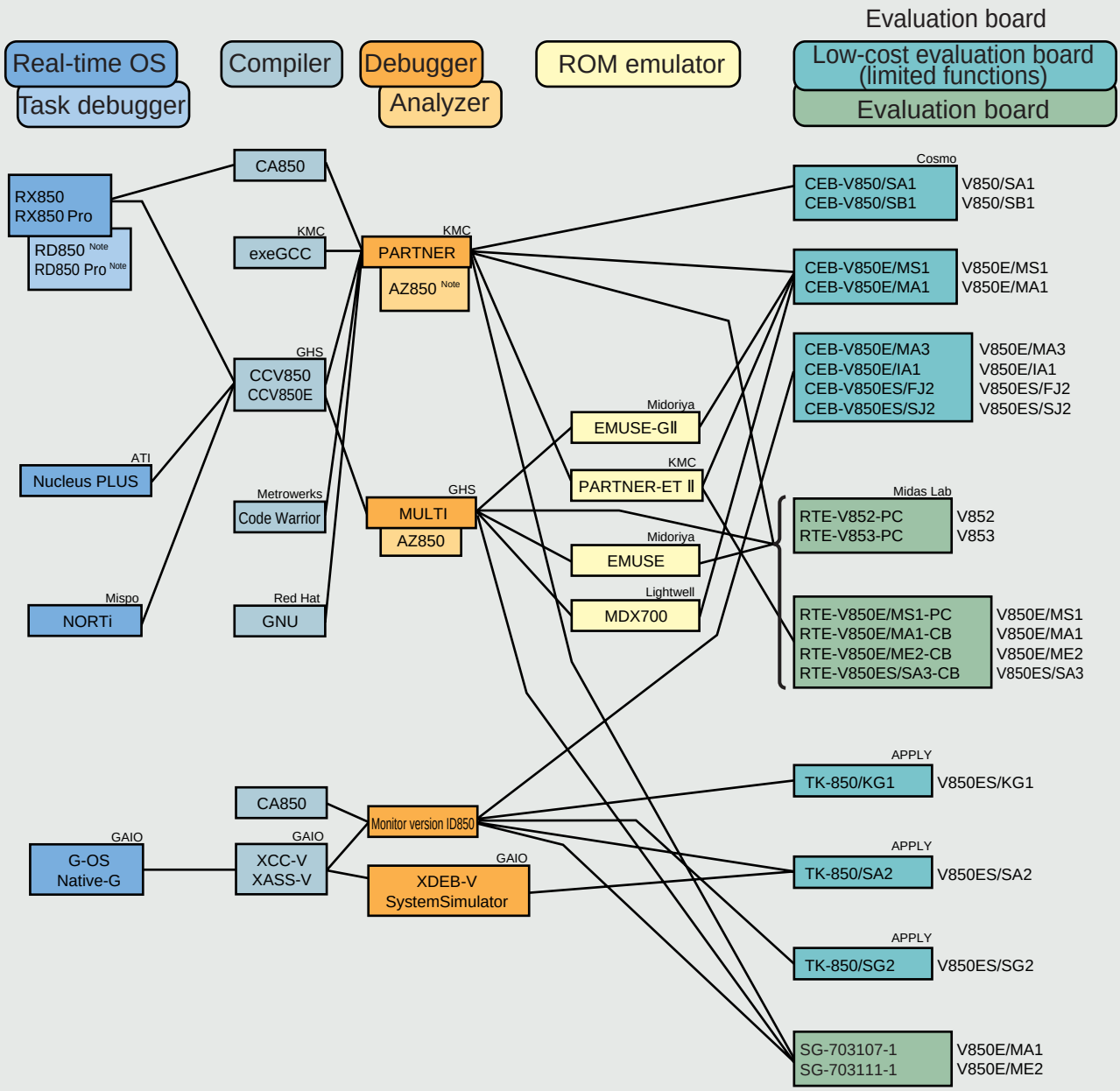


Note The RD850, RD850 Pro, and AZ850 can be used with the ID850, ID850QB, MULTI, PARTNER, and WATCHPOINT.

ATI	:Accelerated Technology, Inc.	Midas Lab	:Midas Lab Co., Ltd.
CATS	:Communication and Technology Systems, Inc.	Mispo	:MiSPO, Inc.
GAIO	:Gaio Technology Co., Ltd.	Red Hat	:Red Hat Corporation
GHS	:Green Hills Software, Inc.	Sophia Systems	:Sophia Systems Co., Ltd.
KMC	:Kyoto Microcomputer Corporation	YDC	:Yokogawa Digital Computer Corporation
Metrowerks	:Metrowerks Corporation	Unmarked	:NEC Electronics

V850 Series Development Environment (2/2)

Development environment using ROM emulator, evaluation board



Note RD850, RD850 Pro, and AZ850 can be used with MULTI, PARTNER.

APPLY	:Application Corporation
ATI	:Accelerated Technology, Inc.
Cosmo	:Cosmo Co., Ltd.
Red Hat	:Red Hat Corporation
GAIO	:Gaio Technology Co., Ltd.
GHS	:Green Hills Software, Inc.
KMC	:Kyoto Microcomputer Corporation
Lightwell	:Lightwell Co., Ltd.
Metrowerks	:Metrowerks Corporation
Midas Lab	:Midas Lab, Co., Ltd.
Midoriya	:Midoriya Electric Co., Ltd.
Mispo	:MiSPO, Inc.
WRS	:Wind River Systems, Inc.
eSOL	:eSOL Co., Ltd.
Unmarked	:NEC Electronics

Software Product

Software package (SP850)

■ Product configuration

The SP850 software package consists of the following software development tools.

- C compiler (CA850)
- Project Manager (PM plus)
- Integrated debugger (ID850, ID850NW) (to be packaged)
- System simulator (SM850, SM plus) (to be packaged)
- Performance analysis tuning tool (TW850)
- Device file (DF703xxx)

C compiler (CA850)

■ Features

- Complies with ANSI-C, a C language standard.
- Supports libraries for embedded systems
- Compact code size and faster execution speed can be realized through powerful optimization
- Utilities useful for embedded systems (ROMization processor, etc.)
- Description of embedded systems in C language (specification of memory allocation and I/O register access) is possible.

System simulator (SM850, SM plus)

■ Features

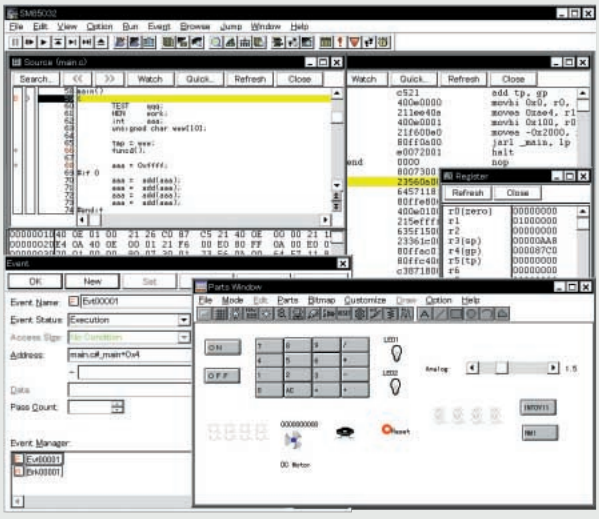
- Same operability as debugger
- Target-less evaluation prior to target completion possible
- In addition to the operation of the CPU itself, target system operation including on-chip peripheral unit and interrupt servicing can also be simulated.
- Pseudo-target system construction and I/O operation are possible through external parts.
- Data generated by 0/1 logic and timing charts can be input to the program being simulated.
- Larger number of events than in-circuit emulator
- Execution speed estimates can be done on the host machine to accurately simulate pipeline operation[Note].
- Construction by user target system users is possible through user open interface.
- A peripheral I/O register status can be specified and when this status occurs, the system can be made to output an interrupt at the desired timing or transfer data to memory (peripheral I/O register event & action function).

Note The pipeline mode is supported by the V853.

■ Target devices

V853, V850/SA1, V850/SB1, V850/SB2, V850/SF1, V850/SC1, V850/SC2, V850/SC3, V850E/MS1, V850E/MA1, V850E/MA2, V850E/IA1, V850E/IA2, V850ES/SA2, V850ES/SA3, V850ES/KF1, V850ES/KG1, V850ES/KJ1, V850ES/SG2[Note], V850ES/SJ2[Note], V850ES/FE2[Note], V850ES/FF2[Note], V850ES/FG2[Note], V850ES/FJ2[Note]

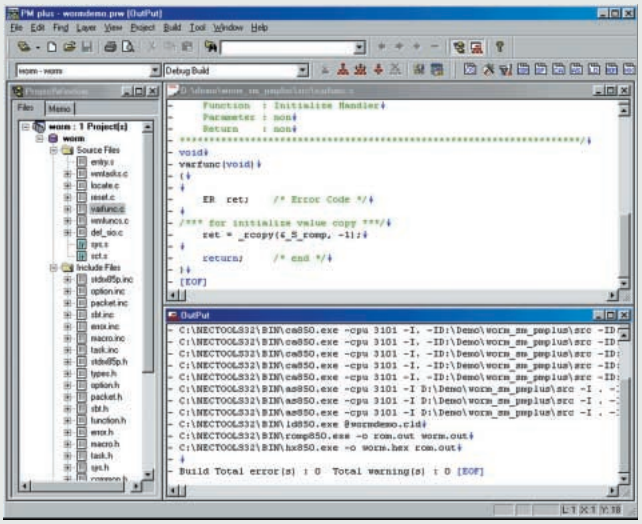
Note Only SM plus is supported



Project manager (PM plus)

■ Features

- Project management (management of target chip, source, and environment during debugging is possible.)
- Supports wizard function during project creation
- Automation of series of operations consisting of edit, build, and debug
- Integration of Help function



N-Wire card (IE-V850E1-CD-NW)

■ Features

- Supports V850E and V850ES
- Emulator for on-chip debugging
- Enables realization of low-cost development environment
- Compact PC card type
- Function for download to internal flash ROM
- Same ease of operation as ID850

■ Target Devices

V850E/ME2, V850E/MA3, V850E/IA4, V850E/SV2, V850ES/SG2, V850ES/SJ2, V850ES/FE2, V850ES/FF2, V850ES/FG2, V850ES/FJ2, V850ES/KJ1, V850ES/KJ1+, µPD70F3229Y

Development Environment

Integrated debugger (ID850, ID850NW, ID850QB)

■ Features

- Supports object files
- Debugging at source level
- Debugging using target resources
- Real-time execution on target
- Event setting according to complex software operation
- Online help function

Real-time OSs (RX850, RX850 Pro)

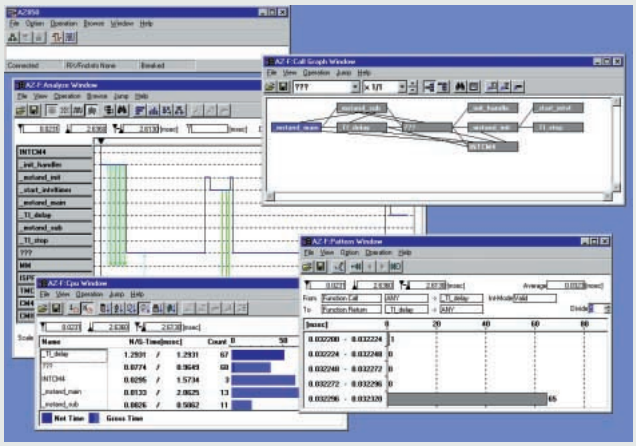
■ Features

- Comply with global standard (µITRON 3.0 specifications).
- Support power management function.
- Enable embedding of required functions only (selection of system calls to be used).
- Support sophisticated task development through task debugger (RD).
- Support application operation analysis through system performance analyzer (AZ)
- Inherit attributes of real-time OS of 16-bit V Series and 78K Series

System performance analyzer (AZ850)

■ Features

- Detection of bugs through system timing errors
- Detection of bugs due to simultaneous operation of complex tasks
- Detection/analysis of real-time system execution performance
- Operation linked to various debuggers



In-circuit emulator (IE, IECUBE)

■ Features

- Emulator functions loaded in dedicated chip to realize high equivalence
- Connectable to variety of computers
- Large array of emulation functions
- Realization of maximum operating frequency equivalent to that of device

Task debuggers (RD850, RD850 Pro)

■ Features

- Display detailed information on OS resources such as tasks.
- Display source of referenced tasks.
- Included with real-time OS (RX850, RX850 Pro)

TCP/IP software library (RX-NET) for V850E products

■ Product configuration

- TCP/IP protocol stack
- Applications
- LAN control driver

■ Features

- RFC-compliant
- Support of numerous socket interfaces/libraries
- Support of applications as option products
- Provided device driver
- Support of NEC Electronics real-time OS (RX850 Pro)

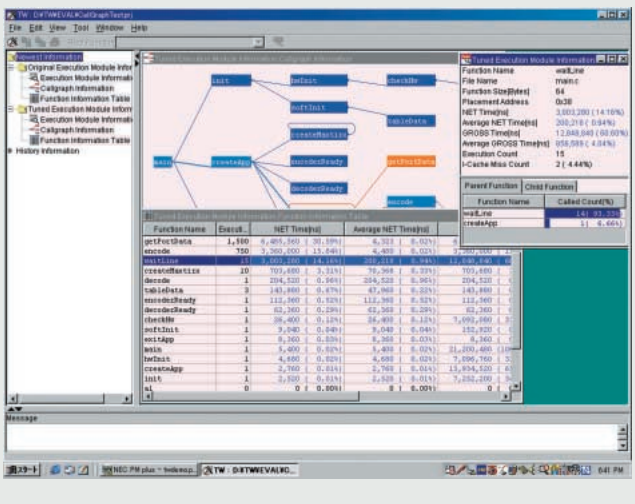
■ Target devices

V850E products

Performance analysis tuning tool (TW850)

■ Features

- Performance analysis changing the internal ROM size, instruction cache size, etc., is possible.
- Display of inter-function call relationships, call count information, function execution time information, and cache mishit information
- Functions optimally placed to reduce cache mishit count
- Functions causing bottlenecks placed into internal ROM or other high-speed access memory



OSEK/VDX specifications compliant OS (RX-OSEK850)

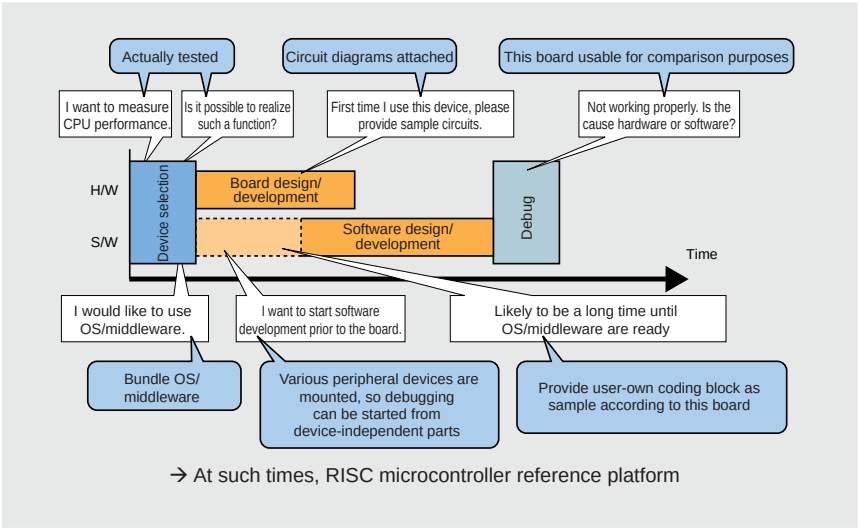
■ Features

- Kernel
  Compliant with OSEK/VDX OS Ver. 2.0 specifications
  Supports 4 conformance classes: BCC1, BCC2, ECC1, and ECC2.
- Configurator
  Configurator (OIL850) allowing easy system information creation provided as standard.
  Configuration files support formats compatible with OIL Ver. 2.0.
- Task debugger (RD-OSEK850)
  Task debugger effective for application debugging using RX-OSEK850 provided as standard

RISC microcontroller reference platform (SolutionGear™)

■ Features

- General-purpose evaluation boards available as RISC microcontroller software development platform
- Target CPU: V850E/MA1, V850E/ME2
- Industry standard PC-compatible interfaces including PCI, ISA, PCMCIA, E-IDE, Ethernet™, Serial, Parallel, PS/2, and USB, provided
- CPU independent motherboards and CPU boards used combined
- Bundled real-time OS, middleware, and sample drivers
- MULTI-PARTNER remote monitor version can be used
- Reference design information provided



→ At such times, RISC microcontroller reference platform

Cooperation with third parties

By deepening cooperation with third-party companies and forming an array of tools combining NEC Electronics-made tools and third-party-made tools, NEC Electronics offers development environments that support the diverse needs of users.

V850 Series Website

Information about V850 microcontrollers and V850 microcontroller development environment can be viewed at the NEC Electronics Microcomputer website.

http://www.necel.com/micro/index_e.html

Microcontroller Search Tool

- Facility for searching for V850 Series microcontrollers by function

Product Lineup

- Microcontroller product information

Document Download

- Microcontroller, development environment, and middleware documents can be downloaded from this area.

  http://www.necel.com/micro/english/document/index.html

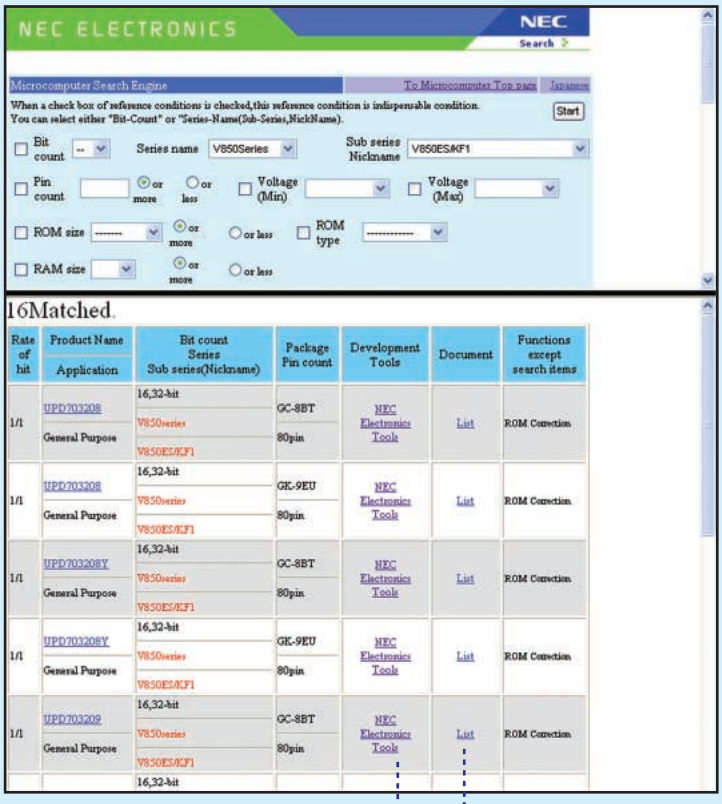
Development Tool Download

- V850 Series development tools can be downloaded from this area. Customers who are registered users receive upgrade information by email.

  http://www.necel.com/micro/ods/eng/index.html

Microcontroller Search Tool

Facility for searching V850 Series microcontrollers by function.



Specify search condition(s) here.

The corresponding NEC Electronics development environment documents can be searched from here with a single link.

Development Tool List

UPD703209GC-8BT Development Tools List

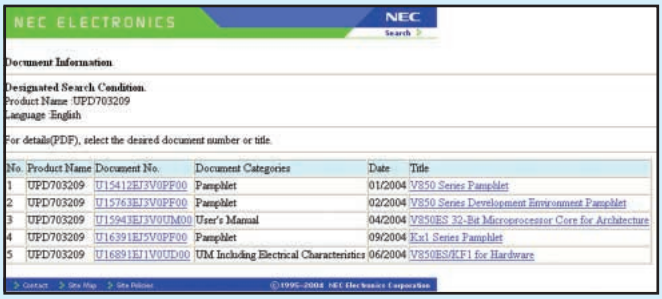
[Software]

Category	Name	Rev	Notes	Document
Software Package	SP850	V3.00	-	List
Device File	DF703210	V1.00	-	List
C-Compiler	CA703000	V2.50	-	List
Assembler	-	-	-	-
Integrated Debugger	ID703000	V2.51	-	List
Integrated Debugger(N-Wire)	-	-	-	-
System Simulator	-	-	-	-
System Performance Analyzer	AZ703000	V3.10	-	List
Real Time OS	RX703000 RX703100	V3.13 V3.13	-	List List

[Hardware]

Category		Name	Rev	Notes	Document
Emulator		IE-V850ES-G1	D	-	List
Emulator (Entry Model)		IE-V850ESK1-ET	A	-	List
N-Wire Emulator		-	-	-	-
Emulation(Option) Board		IE-703217-G1-EM1	B(1.20)	-	List
PC Interface	AT Compatible (PCI-Bus)	IE-70000-PCI-IF-A	B	-	-
	Note-PC (PCMCIA)	IE-70000-CD-IF-A	A	-	-

Document Information List



Product Lineup

MEMO

MEMO

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