Ei16C550 FIFO UART



FEATURES

- ï 5V Operation
- ï Full duplex asynchronous receiver and transmitter
- Easily interfaces to most popular microprocessors
- ï Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- i Independently controlled transmitter, receiver, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2¹⁶-1) and generates the internal 16 x clock
- i Independent receiver clock input
- ii MODEM control functions (CTS, RTS, DSR, DTR, RI,and DCD)
- Fully programmable serial interface characteristics:
 - 5, 6, 7, or 8 bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1, 1.5, or 2 stop bit generation
 - Baud generation (DC to 56k baud)
- ï False start bit detection
- ï Complete status reporting capabilities

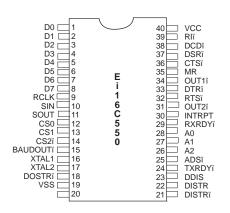
- Tri-StateÆTTL drive capabilities for bidirectional data bus and control bus
- i Line break generation and detection
- ï Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation
 - Break, parity overrun, and framing error simulation
- ï Fully prioritized interrupt systems controls
- i 16 byte FIFO for reduced CPU overhead

DESCRIPTION

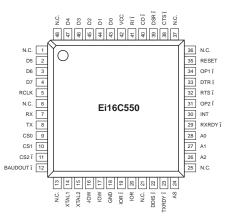
The Epic Ei16C550 Universal Asynchronous Receiver Transmitter (UART) is a CMOS-VLSI communication device in a single package.

The UART performs serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversions on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operation being performed by the UART, as well as any error conditions (party, overrun, framing, or break detect).

PIN CONFIGURATION



D4 D3 D1 D0 NC VCC VCC VCC CDI DCDI CTSI MR D5 D6 D7 RCLK OUT1ï DTRï 38 37 8 9 10 11 12 13 14 15 16 17 RTSï 36 34 33 32 31 30 29 OUT2ï NC SIN NC SOUT Fi16C550 INTRPT RXRDYï CS0 CS1 CS2ï A1 A2 BAUD-



40-PIN DIP

44-PIN PLCC

48-PIN TQFP



The UART includes a programmable baud generator which is capable of dividing the timing reference clock input by divisors of 1 to (2¹⁶-1), and producing a 16 x clock to drive the receiver logic. Also included in the

UART is a complete MODEM control capability, and processor interrupt system that may be software tailored to the users requirement to minimize the computing needed to handle the communications link.

BLOCK DIAGRAM

