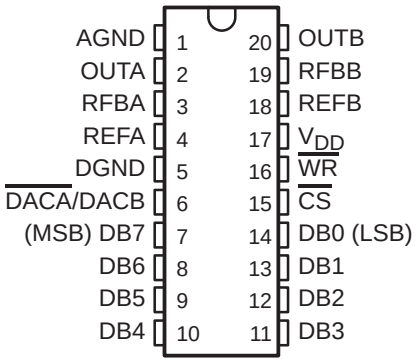
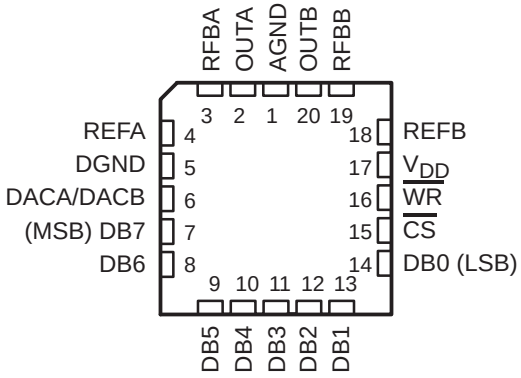
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Interchangeable With Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320**
- **Voltage-Mode Operation**
- **CMOS Technology**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	20 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay Time at V_{DD} = 5 V	80 ns

DW, N OR PW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC7528C, TLC7528E, and TLC7528I are dual, 8-bit, digital-to-analog converters designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit, input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is to be loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

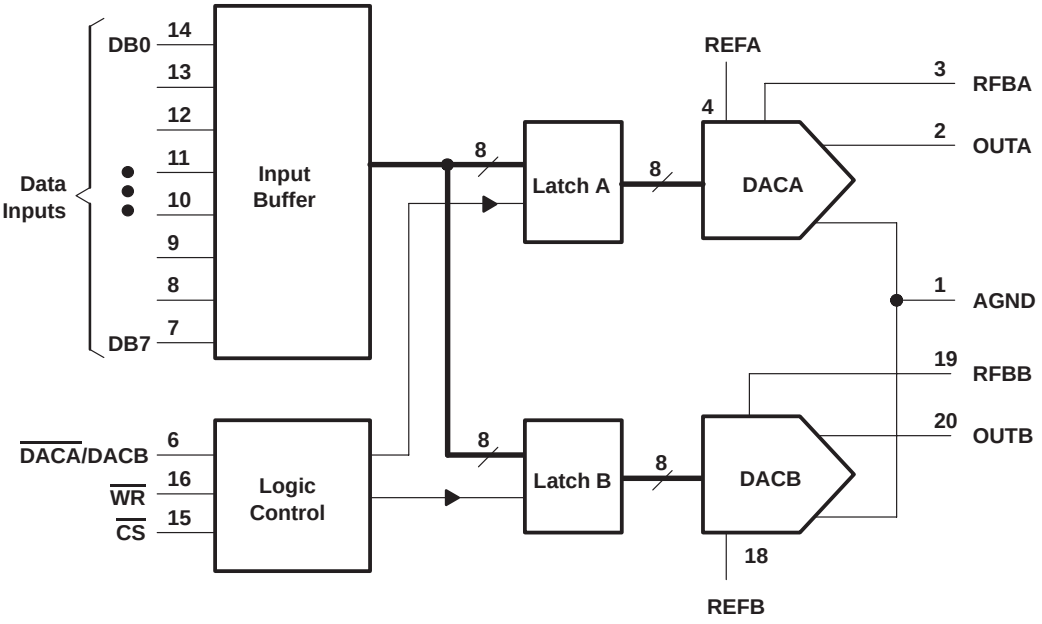
These devices operate from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). The 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application information in this data sheet.

The TLC7528C is characterized for operation from 0°C to 70°C. The TLC7528I is characterized for operation from –25°C to 85°C. The TLC7528E is characterized for operation from –40°C to 85°C.

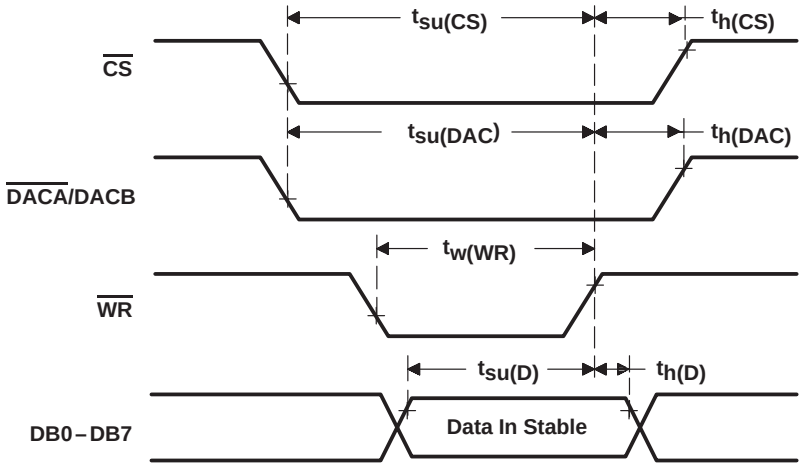
AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)	SMALL OUTLINE (PW)
0°C to 70°C	TLC7528CDW	TLC7528CFN	TLC7528CN	TLC7528CPW
–25°C to 85°C	TLC7528IDW	TLC7528IFN	TLC7528IN	TLC7528IPW
–40°C to 85°C	TLC7528EDW	TLC7528EFN	TLC7528EN	TLC7528EPW

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (to AGND or DGND) . . . . . –0.3 V to 16.5 V
Voltage between AGND and DGND . . . . . $\pm V_{DD}$
Input voltage range, V_I (to DGND) . . . . . –0.3 V to V_{DD} + 0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Input voltage (voltage mode out A, out B to AGND) . . . . . –0.3 V to V_{DD} + 0.3
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range, T_A: TLC7528C . . . . . 0°C to 70°C
TLC7528I . . . . . –25°C to 85°C
TLC7528E . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7628C	0		70	0		70	°C
	TLC7628I	–25		85	–25		85	
	TLC7628E	–40		85	–40		85	

electrical characteristics over recommended operating free-air temperature range, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		$V_I = 0$	5	12	–10	5	12	–10	μA
	Reference input impedance REFA or REFB to AGND					20			20	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V			±400			±200	nA
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, Δgain/ΔV_{DD}		$\Delta V_{DD} = \pm 10\%$			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		All digital inputs at V_{IH}min or V_{IL}max			2			2	mA
I_{DD}	Supply current (standby)		All digital inputs at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0–DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$, DACA/DACB				15			15	pF
C_o	Output capacitance (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

† All typical values are at $T_A = 25°C$.

operating characteristics over recommended operating free-air temperature range, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			–65			–65	dB
	REFB to OUTB				–65			–65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nV•s
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C		–85			–85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = V_{ref} – 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. $V_{refA} = V_{refB}$ = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

PRINCIPLES OF OPERATION

These devices contain two identical, 8-bit-multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_o is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 50 pF to 120 pF maximum. The equivalent output resistance (r_o) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

PRINCIPLES OF OPERATION

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 5 V. These devices can operate with any supply voltage in the range from 5 V to 15 V; however, input logic levels are not TTL compatible above 5 V.

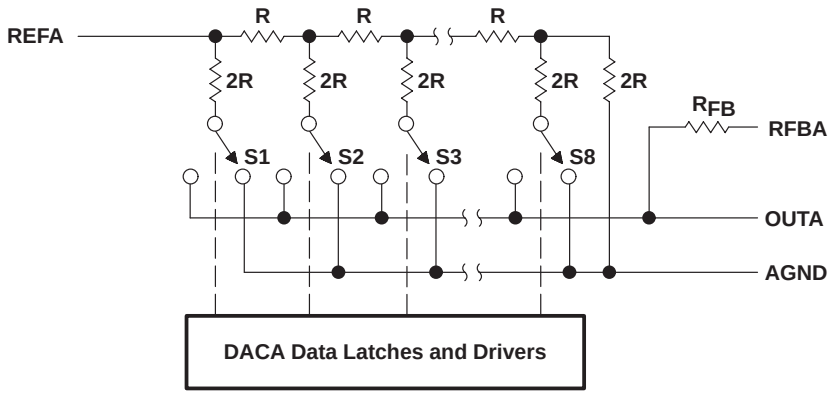


Figure 1. Simplified Functional Circuit for DACA

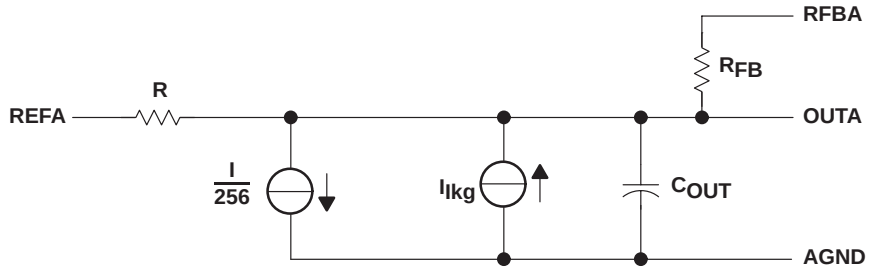


Figure 2. TLC7528 Equivalent Circuit, DACA Latch Loaded With 11111111

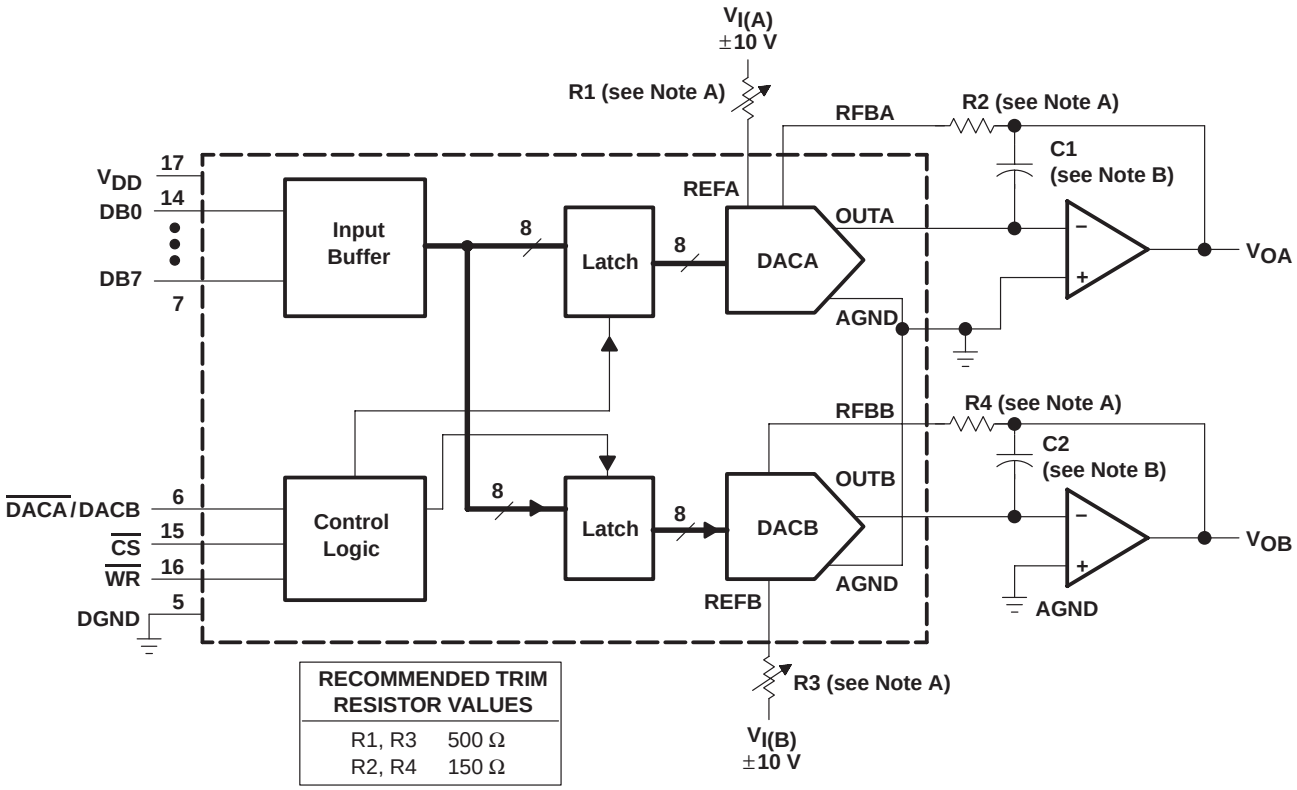
MODE SELECTION TABLE

$\overline{\text{DACA}}$/DACB	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

APPLICATION INFORMATION

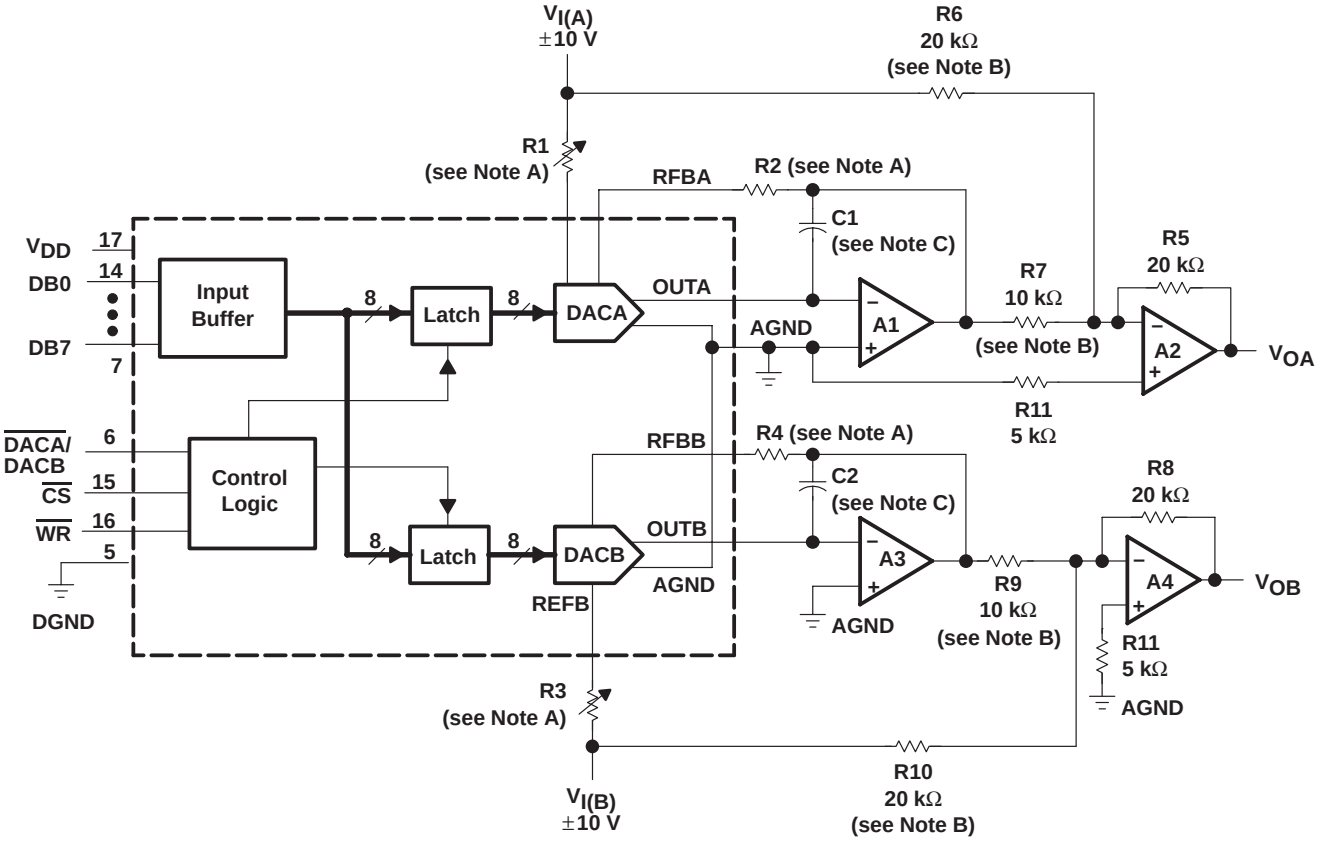
These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation.



NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)

APPLICATION INFORMATION



NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_I$ (255/256)
1 0 0 0 0 0 0 1	$-V_I$ (129/256)
1 0 0 0 0 0 0 0	$-V_I$ (128/256) = $-V_I/2$
0 1 1 1 1 1 1 1	$-V_I$ (127/256)
0 0 0 0 0 0 0 1	$-V_I$ (1/256)
0 0 0 0 0 0 0 0	$-V_I$ (0/256) = 0

†1 LSB = $(2^{-8})V_I$

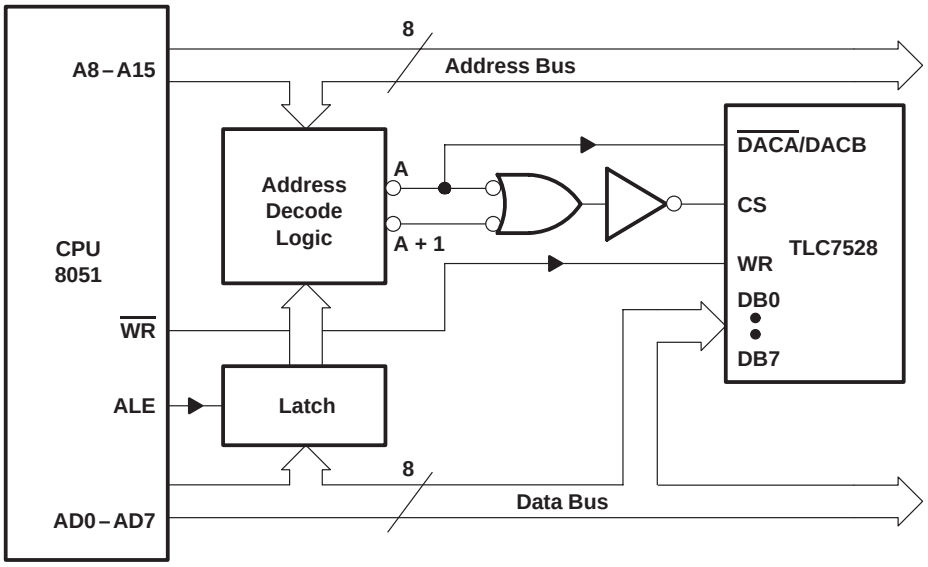
Table 2. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
1 1 1 1 1 1 1 1	V_I (127/128)
1 0 0 0 0 0 0 1	V_I (1/128)
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$-V_I$ (1/128)
0 0 0 0 0 0 0 1	$-V_I$ (127/128)
0 0 0 0 0 0 0 0	$-V_I$ (128/128)

‡1 LSB = $(2^{-7})V_I$

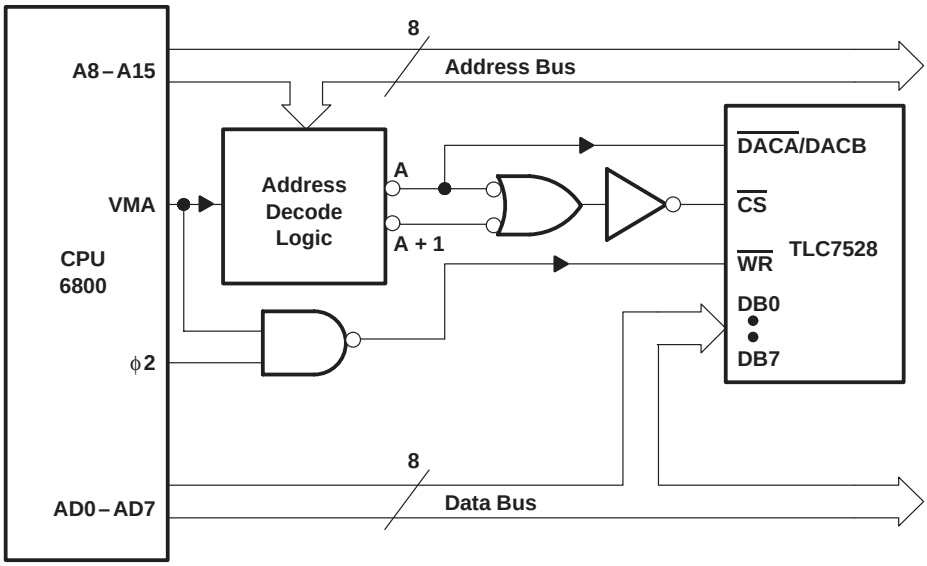
APPLICATION INFORMATION

microprocessor interface information



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

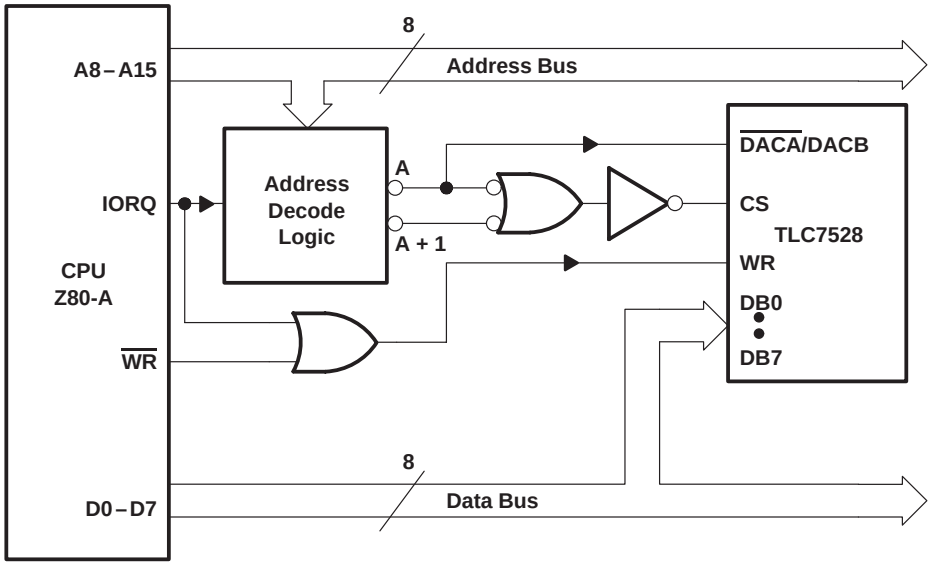
Figure 5. TLC7528 – Intel 8051 Interface



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

Figure 6. TLC7528 – 6800 Interface

APPLICATION INFORMATION



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

Figure 7. TLC7528 To Z-80A Interface

programmable window detector

The programmable window comparator shown in Figure 8 determines if voltage applied to the DAC feedback resistors are within the limits programmed into the data latches of these devices. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits drives the output high.

APPLICATION INFORMATION

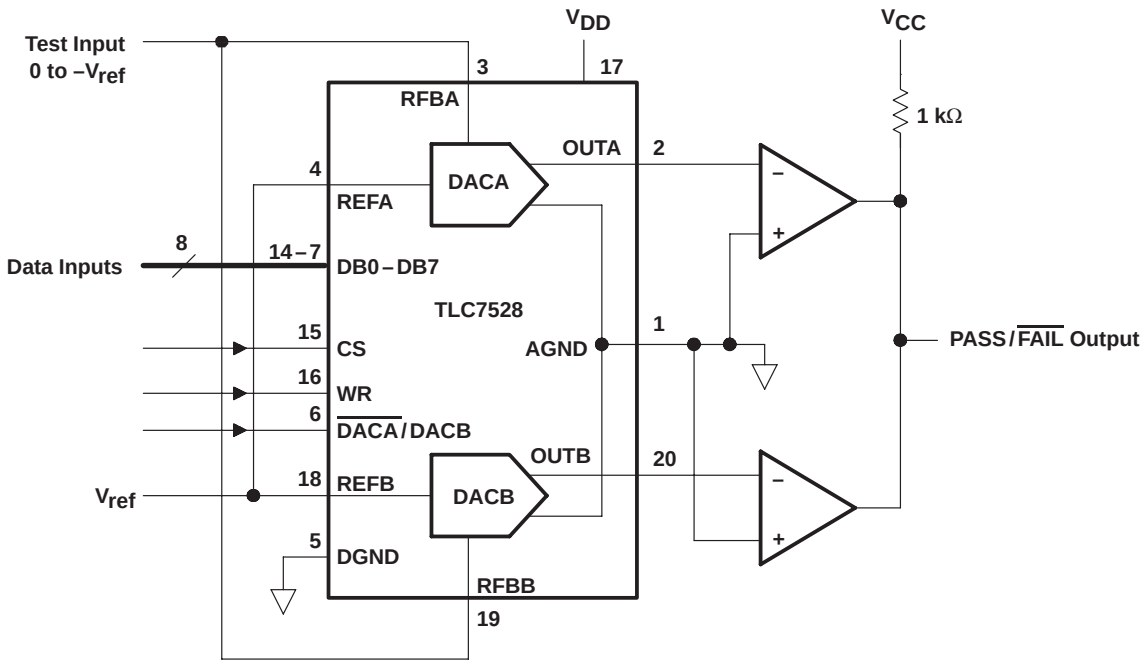


Figure 8. Digitally-Programmable Window Comparator (Upper- and Lower-Limit Tester)

digitally controlled signal attenuator

Figure 9 shows a TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

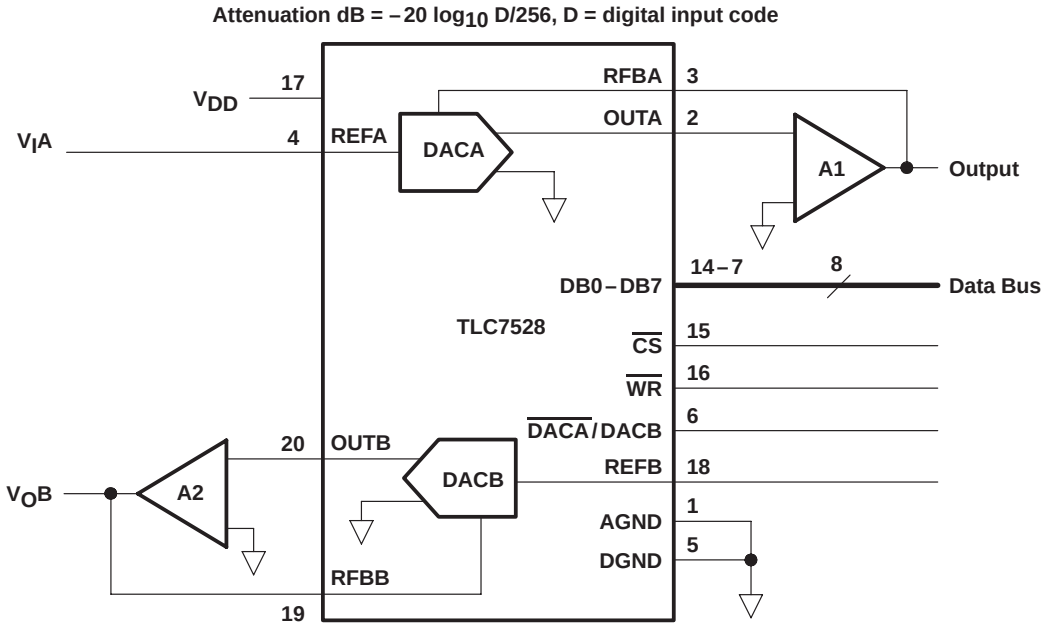


Figure 9. Digitally Controlled Dual Telephone Attenuator

APPLICATION INFORMATION

Table 3. Attenuation vs DACA, DACB Code

ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 1 1 1 1	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

programmable state-variable filter

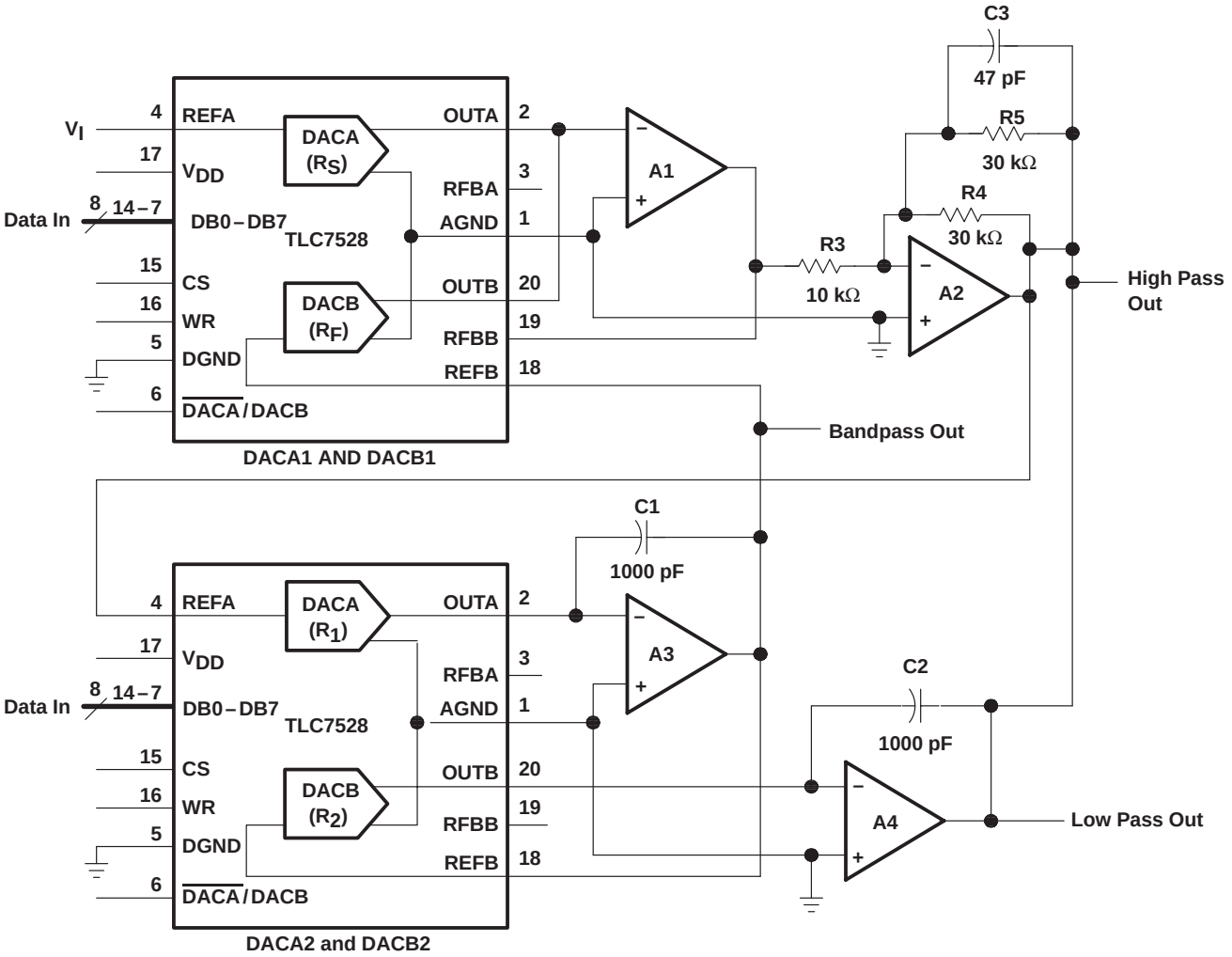
This programmable state-variable or universal filter configuration provides low-pass, high-pass, and bandpass outputs, and is suitable for applications requiring microprocessor control of filter parameters.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easy to achieve.

$$f_c = \frac{1}{2\pi\ R1C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.

APPLICATION INFORMATION



Circuit Equations:

$C_1 = C_2$, $R_1 = R_2$, $R_4 = R_5$

$$Q = \frac{R_3}{R_4} \times \frac{R_F}{R_{fb(DACB1)}}$$

Where:

R_{fb} **is the internal resistor connected between OUTB and RFBB**

$$G = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.
B. CS compensates for the op-amp gain-bandwidth limitations.
C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

Figure 10. Digitally Controlled State-Variable Filter

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current multiplying D/A converter of these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 11 is an example of a current multiplying D/A, that operates in the voltage mode.

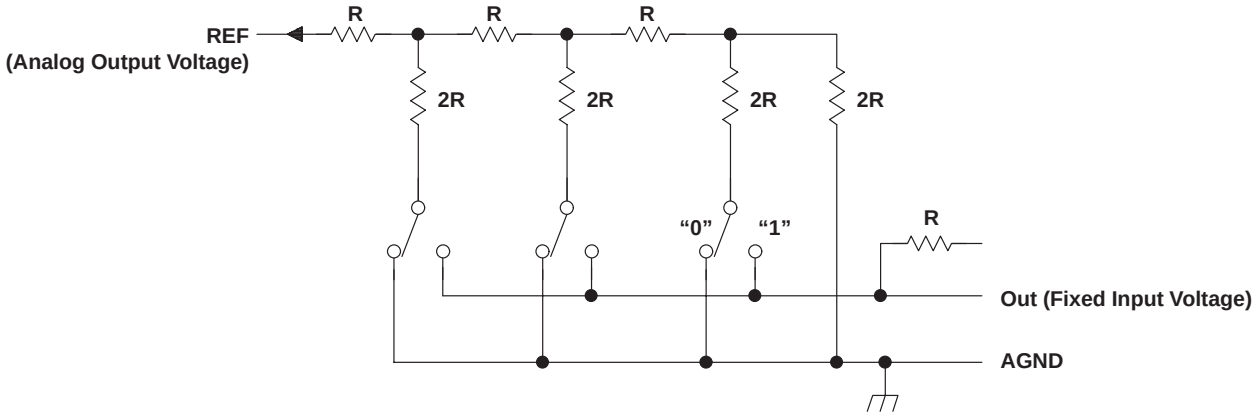


Figure 11. Voltage-Mode Operation

The following equation shows the relationship between the fixed input voltage and the analog output voltage:

$$V_O = V_I (D/256)$$

Where:

V_O = analog output voltage
V_I = fixed input voltage (must not be forced below 0 V.)
D = digital input code converted to decimal

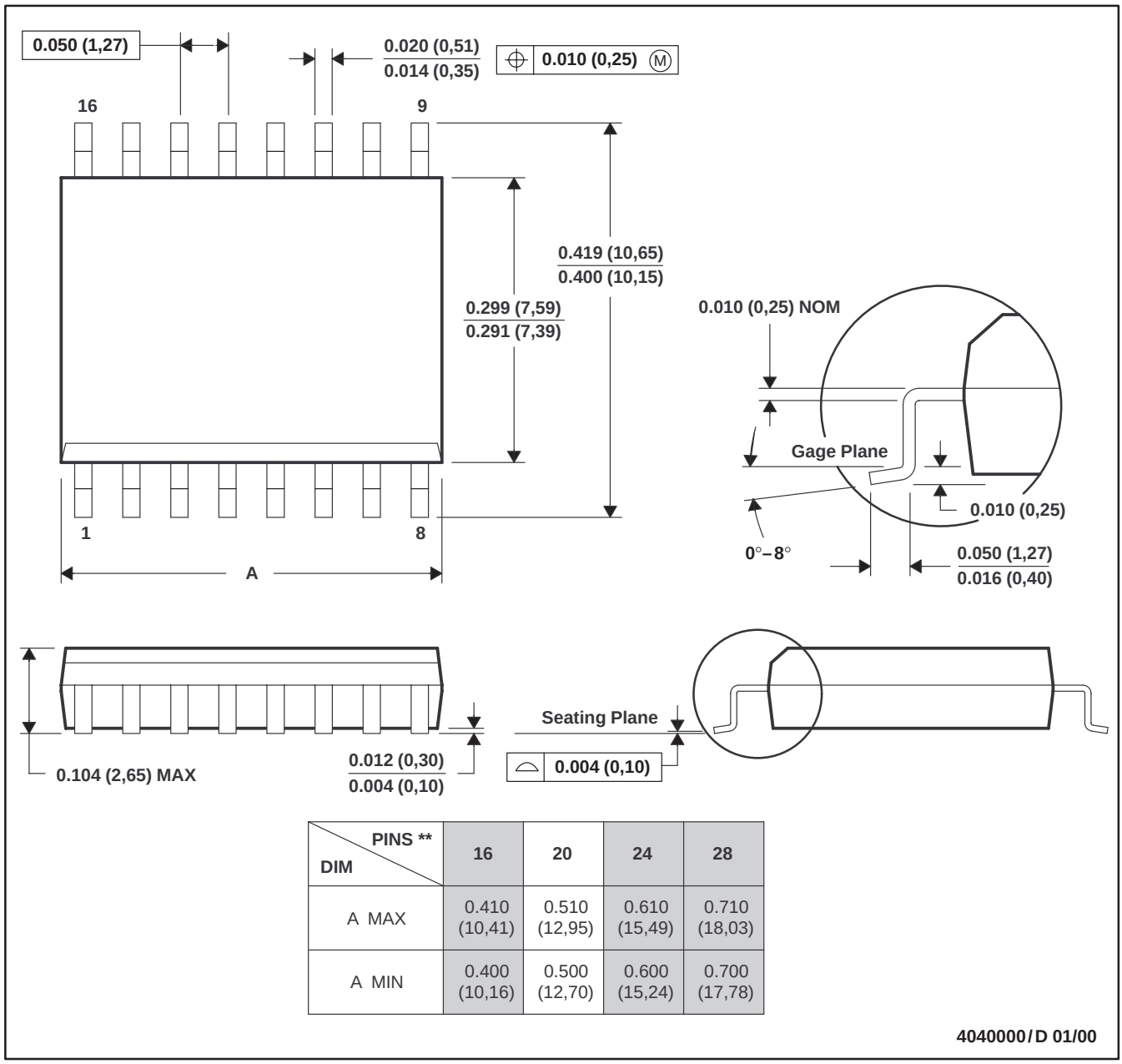
In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REFA or REFB	V_{DD} = 5 V, OUTA or OUTB at 2.5 V, T_A = 25°C		1	LSB

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/D 01/00

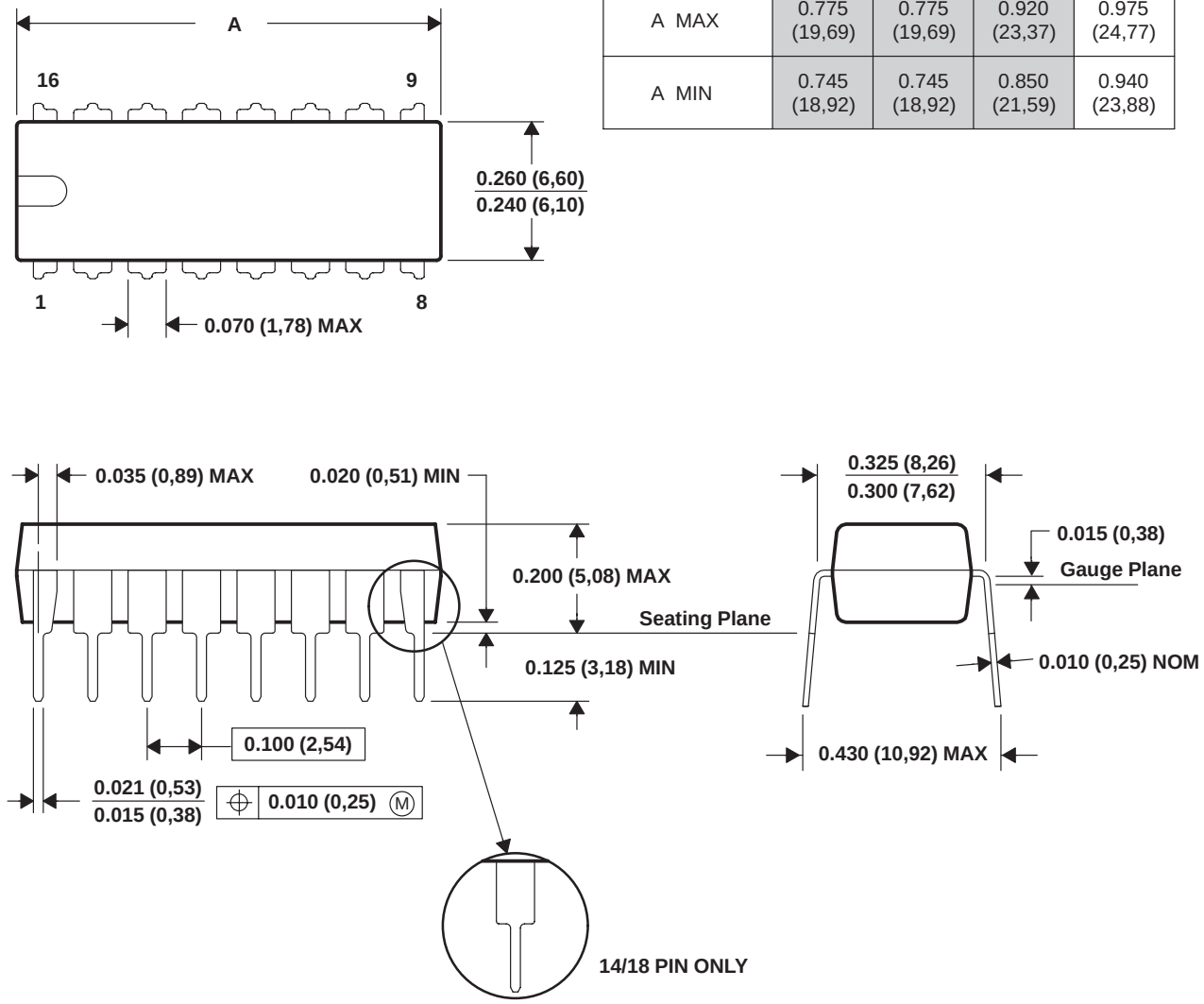
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

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